Graphics 8
Graphics Hardware - 1469 Gear

by

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December 1969

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Graphics 8

Introduction

This report was written for two reasons. The first was to serve as a reference manual for the 1469 group in their everyday graphics work. The second was to serve as an applications manual for use by those University people who make use of the graphics facility.

The report is divided into three parts: basic system, operating additions, and proposed additions. The basic system made up of a 16K-PDP-8 with interval timer, an ASR33 Teletype, 2 ea Dectapes, and a PDB-338 was installed and checked-out in June of 1967. The operating additions have been made over the past two years. The proposed additions are being worked-on for purposes of making the total facility better for user applications.

The items that make up the individual parts are described in this report and/or reference is made to another report for a more detailed description.

Figure 1 is a configuration drawing of the Graphics 8 hardware. The four quadrants contain devices, controllers or interfaces corresponding to the title of the quadrant. The three communication interfaces have been particularly useful in enhansing the PDP-8 capabilities for graphics developments and user applications. The Graphics (system) is the present basic system tools for graphic work on the PDP-8. The Graphics (applications) is the developmental project for expanding the user facilities of the PDP-8. The local I/Ø contains the various low-speed devices accessable to the user at the PDP-8.

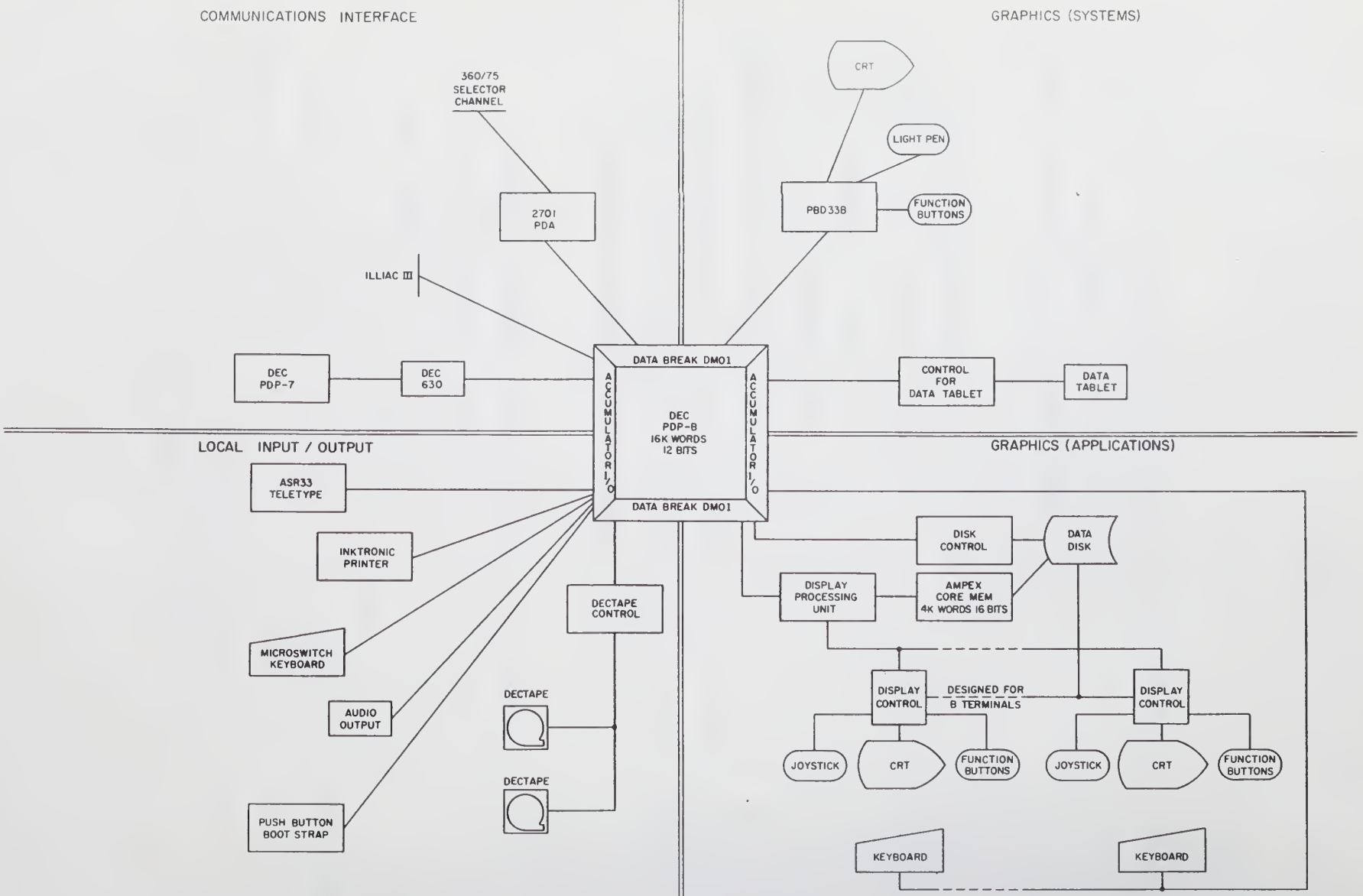

COMMUNICATIONS INTERFACE
GRAPHICS (SYSTEMS)
360/75 SELECTOR CHANNEL
2701 PDA
ILLIAC III
DEC PDP-7
DEC 630
CRT
LIGHT PEN
PBD338
FUNCTION BUTTONS
DATA BREAK DMO1
ACCUMULATOR I/O
DEC PDP-8 16K WORDS 12 BITS
ACCUMULATOR I/O
DATA BREAK DMO1
CONTROL FOR DATA TABLET
DATA TABLET
LOCAL INPUT / OUTPUT
GRAPHICS (APPLICATIONS)
ASR33 TELETYPE
INKTRONIC PRINTER
MICROSWITCH KEYBOARD
AUDIO OUTPUT
PUSH BUTTON BOOT STRAP
DECTAPE CONTROL
DECTAPE
DECTAPE
DISK CONTROL
DATA DISK
DISPLAY PROCESSING UNIT
AMPEX CORE MEM 4K WORDS 16 BITS
DISPLAY CONTROL
DESIGNED FOR 8 TERMINALS
DISPLAY CONTROL
JOYSTICK
CRT
FUNCTION BUTTONS
JOYSTICK
CRT
FUNCTION BUTTONS
KEYBOARD
KEYBOARD

figure 1

Basic System

The graphics 8 was ordered as a stand-alone graphics system with the PDP-8 processor, ASR33 teletype, 338 programmed buffered display, dectapes, and interval timer. This section of the report is made-up of short descriptions of each of these five pieces of the basic system.

The Digital Equipment Corporation Programmed Data Processor-8 (PDP-8) is designed for use as a small-scale general-purpose computer, an independent information handling facility in a large computer system, or as the control element in a complex processing system. The PDP-8 is a one-address, fixed word length, parallel computer using 12 bit, two's complement arithmetic. Cycle time of the 16K word random-address magnetic-core memory is 1.5 microseconds. Standard features of the system include indirect addressing and facilities for instruction skipping and program interruption as functions of input-output device conditions.

Flexible, high-capacity, input-output capabilities of the computer allow it to operate a variety of peripheral equipment. In addition to standard Teletype and performatted tape equipment, the system is capable of operating in conjunction with a number of optional devices such as high-speed perforated tape readers and punches, card equipment, a line printer, analog-to-digital converters, cathode-ray-tube displays, magnetic drum systems, and magnetic-tape equipment. Equipment of special design is easily adapted for connection into the PDP-8 system.

COMPUTER ORGANIZATION

The PDP-8 system is organized into a processor, core memory, and input/output equipment and facilities. All arithmetic, logic, and system control operations of the standard PDP-8 are performed by the processor. Permanent (longer than one instruction time) local information storage and retrieval operations are performed by the core memory. The memory is continuously cycling and automatically performing a read and write operation during each computer cycle. Input and output address and data buffering

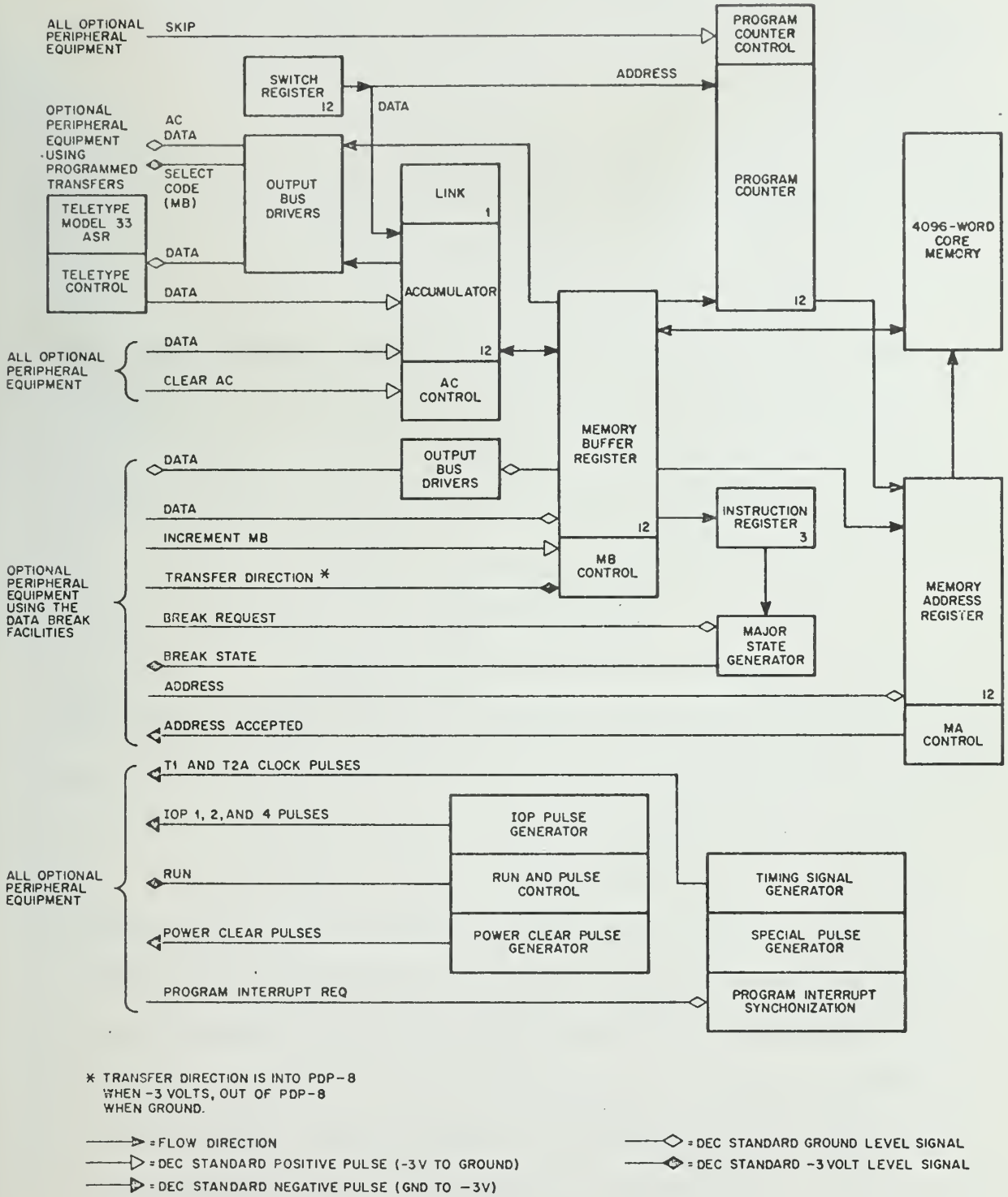


Fig. 2 PDP-8 Block Diagram

for the core memory is performed by registers of the processor, and operation of the memory is under control of timing signals produced by the processor.

Interface circuits for the processor allow bussed connections to a variety of peripheral equipment. Each input/output device is responsible for detecting its own select code and for providing any necessary input or output gating. Individually programmed data transfers between the processor and peripheral equipment take place through the processor accumulator. Data transfers can be initiated by peripheral equipment rather than by the program, by means of the data break facilities. Standard features of the PDP-8 also allow peripheral equipment to perform certain control functions such as instruction skipping and a transfer of program control initiated by a program interrupt.

MAJOR REGISTERS

To store, retrieve, control, and modify information and to perform the required logical, arithmetic, and data processing operations, the core memory and the processor employ the logic components shown in Figure 2 and described in the following paragraphs.

Accumulator (AC)

Arithmetic and logic operations are performed in this 12-bit register. Under program control the AC can be cleared or complemented, its content can be rotated right or left with the link. The content of the memory buffer register can be added to the content of the AC and the result left in the AC. The content of both of these registers may be combined by the logical operation AND, the result remaining in the AC. The memory buffer register and the AC also have gates which allow them to be used together as the shift register and buffer register of a successive approximation

analog-to-digital converter. The inclusive OR may be performed between the AC and the switch register on the operator console and the result left in the AC.

The accumulator also serves as an input-output register. All programmed information transfers between core memory and an external device pass through the accumulator.

Link (L)

This one-bit register is used to extend the arithmetic facilities of the accumulator. It is used as the carry register for two's complement arithmetic. Overflow into the L from the AC can be checked by the program to greatly simplify and speed up single and multiple precision arithmetic routines. Under program control the link can be cleared and complemented, and it can be rotated as part of the accumulator.

Program Counter (PC)

The program sequence, that is the order in which instructions are performed, is determined by the PC. This 12-bit register contains the address of the core memory location from which the next instruction will be taken. Information enters the PC from the core memory, via the memory-buffer register, and from the switch register on the operator console. Information in the PC is transferred into the memory address register to determine the core memory address from which each instruction is taken. Incrementation of the content of the PC establishes the successive core memory locations of the program and provides skipping of an instruction based upon a programmed test of information or conditions.

Memory Address Register (MA)

The address in core memory which is currently selected for reading

or writing is contained in this 12-bit register. Data can be set into it from the memory buffer register, from the program counter, or from an I/O device using the data break facilities.

Switch Register (SR)

Information can be manually set into the switch register for transfer into the PC as an address by means of the LOAD ADDRESS key, or into the AC as data to be stored in core memory by means of the DEPOSIT key.

Core Memory

The core memory provides storage for instructions to be performed and information to be processed or distributed. This random address magnetic core memory holds 16K 12-bit words. Memory location 0_8 is used to store the content of the PC following a program interrupt, and location 1_8 is used to store the first instruction to be executed following a program interrupt. (When a program interrupt occurs, the content of the PC is stored in location 0_8 and program control is transferred to location 1 automatically.) Locations 10_8 through 17_8 are used for auto-indexing. All other locations can be used to store instructions or data.

Core memory contains numerous circuits such as read-write switches, address decoders, inhibit drivers, and sense amplifiers. These circuits perform the electrical conversions necessary to transfer information into or out of the core array and perform no arithmetic or logic operations upon the data.

Memory Buffer Register (MB)

All information transfers between the processor registers and the core memory are temporarily held in the MB. Information can be transferred into the MB from the accumulator or memory address register. The MB can be cleared, incremented by one or two, or shifted right. Information can

be set into the MB from an external device during a data break or from core memory, via the sense amplifiers. Information is read from a memory location in 0.8 microsecond and rewritten in the same location in another 0.8 microsecond of one 1.6 microsecond memory cycle.

Instruction Register (IR)

This 3-bit register contains the operation code of the instruction currently being performed by the machine. The three most significant bits of the current instruction are loaded into the IR from the memory buffer register during a Fetch cycle. The content of the IR is decoded to produce the eight basic instructions, and affect the cycles and states entered at each step in the program.

Major State Generator

One or more major control states are entered to determine and execute an instruction. The major state generator determines the machine state during each computer cycle. The major states are Fetch, Defer, Execute, and Break. Each state is produced as a function of the current instruction and the current state, except for the Break state which is entered upon receipt of the Break Request signal supplied by peripheral equipment.

Fetch

During this state an instruction is read into the MB from core memory at the address specified by the content of the PC. The instruction is restored in core memory and retained in the MB. The operation code of the instruction is transferred into the IR to cause enactment, and the content of the PC is incremented by one.

If a multiple-cycle instruction is fetched, the following major state will be either Defer or Execute. If a one-cycle instruction is fetched, the operations specified are performed during the last part of the Fetch cycle and the next state will be another Fetch.

Defer

When a 1 is present in bit 3 of a memory reference instruction, the Defer state is entered to obtain the full 12-bit address of the operand from the address in the current page or page 0 specified by bits 4 through 11 of the instruction. The process of address deferring is called indirect addressing because access to the operand is addressed indirectly, or deferred, to another memory location.

Execute

This state is entered for all memory reference instructions except jump. During an AND, two's complement add, or increment and skip if zero instruction the content of the core memory location specified by the address portion of the instruction is read into the MB and the operation specified by bits 0 through 2 of the instruction is performed. During a deposit and clear accumulator instruction the content of the AC is transferred into the MB and is stored in core memory at the address specified in the instruction. During a jump to subroutine instruction this state occurs to write the content of the PC into the core memory address designated by the instruction and to transfer this address into the PC to change control.

Break

When this state is established, the sequence of instructions is broken for a data break. The break occurs at the completion of the current instruction. The data break allows information to be transferred between core memory and an external device, via the MB. When this transfer has been completed, the program sequence is resumed from the point of the break.

Output Bus Drivers

Output signals from the computer processor are power amplified by output bus driver modules of the standard PDP-8; allowing these signals to drive a heavy circuit load.

Functional Summary

Operation of the computer is accomplished on a limited scale by keys on the operator console. Operation in this manner is limited to address and data storage by means of the switch register, core memory data examination, the normal start/stop/continue control, and the single step or single instruction operation that allows a program to be monitored visually as a maintenance operation. Most of these manually initiated operations are performed by executing an instruction in the same manner as by automatic programming, except that the gating is performed by special pulses rather than by the normal clock pulses. In automatic operation, instructions stored in core memory are loaded into the memory buffer register and executed during one or more computer cycles. Each instruction determines the major control states that must be entered for its execution. Each control state lasts for one 1.5-microsecond computer cycle and is divided into distinct time states which can be used to perform sequential logical operations. Performance of any function of the computer is controlled by gating of a specific instruction during a specific major control state and a specific time state.

TIMING AND CONTROL ELEMENTS

Figure 2 shows the timing and control elements described in the succeeding paragraphs and indicates their relationship to the major registers. These elements can be grouped categorically into timing generators, register controls, and program controls.

Timing Generators

Timing pulses used to determine the computer cycle time and used to initiate sequential time-synchronized gating operations are produced

by the timing signal generator. Timing pulses used during operations resulting from the use of the keys and switches on the operator console are produced by the special pulse generator. Pulses that reset registers and control circuits during power turn on and turn off operations are produced by the power clear pulse generator. Several of these pulses are available to peripheral devices using programmed or data break information transfers.

Register Controls

Operation of the AC, MA, MB, and PC is controlled by an associated logic circuit. These circuits, in turn, transmit and receive control signals to and from I/O equipment. Programmed data transfer equipment can supply a pulse to the AC control to clear the AC prior to a data input and can supply a pulse to cause the content of the PC to be incremented, thus initiating an instruction skip. Equipment using the data break facility passes signals with the MA control and MB control to determine the direction and timing of data transfers in this mode.

Program Controls

Circuits are also included in the PDP-8 that produce the I/O pulses which initiate operations involved in input/output transfers, determine the advance of the computer program, and allow peripheral equipment to cause a program interrupt of the main computer program to transfer program control to a subroutine which performs some service for the I/O device.

INTERFACE

The input/output portion of the PDP-8 is very flexible and interfaces readily with special equipment, especially in real time data processing and control environment.

The PDP-8 utilizes a "bus" I/O system rather than the more conventional "radial" system. The "bus" system allows a single set of data and control

lines to communicate with all I/O devices. The bus simply goes from one device to the next. No additional connections to the computer are required.

External devices receive two types of information from the computer: data and control signals. Computer output data is present as static levels on 12 lines. These levels represent a 12-bit word to be transmitted in parallel to a device. Data signals are received at all devices but are sampled only by the appropriate one in response to a control signal. Control signals are of two types: levels and timing pulses. Six static levels and their complement are supplied by the MB on 12 lines. These lines contain a code representing the device from which action is required. Each device recognizes its own code and performs its function only when this code is present. There are three timing pulses which may be programmed to occur. These IOP pulses are separated in time by one microsecond and are brought to all devices on 3 lines. These pulses are used by a device only when it is selected by the appropriate code on the level lines. They may be used to perform sequential functions in an external register, such as clear and read, or any other function requiring one, two, or three sequential pulses.

Peripheral devices transmit information to the computer on four types of "busses". These are the information bus, the clear AC bus, the skip bus, and the program interrupt bus. The information bus consists of 12 lines normally held at -3 volts by load resistors within the computer. Whenever one of these lines is brought to ground, a binary 1 will be placed in the corresponding accumulator bit. Each device may use the input bus only when it is selected; and thus, these input lines are time shared among all of the connected devices. The skip bus is electrically identical to the information bus. However, when it is driven to ground the next sequential instruction will be skipped. It too can be used only by the device currently

selected and is effectively time shared. The program interrupt bus may be driven to ground at any time by any device whether currently selected or not. When more than one device is connected to the interrupt bus they should also be connected to the skip bus so the program can identify the device requesting program interruption.

The transmission of device slection levels and timing pulses is completely under program control. A single instruction can select any one of 64 devices and transmit up to three IOP timing pulses. Since the timing pulses are individually programmable, one might be used to strobe data into an external device buffer, another to transmit data to the computer, and the third to test a status flip-flop and drive the skip bus to ground if it is in the enabling state.

Data transfers may also be made directly with core memory at a high speed using the data break facility. This is a completely separate I/O system from the one described previously. It is standard equipment in every PDP-8 and is ordinarily used with fast I/O devices such as magnetic drums or tapes. Transfers through the data break facility are interlaced with the program in progress. They are initiated by a request from the peripheral device and not by programmed instruction. Thus, the device may exchange a word with memory whenever it is ready and does not have to wait for the program to issue an instruction. Computation may proceed on an interlaced basis with these transfers.

ASR33 (See Figure 3)

Teletype Corporation Model 33TY Standard Duty Automatic Send-Receive Page Printer Set with Tape Perforator and Reader (Private Line Version) has the following features:

Eight-level, 11.0 unit code (1.0 unit start and 2.0 unit stop pulse)

8-1/2" sprocket feed platen with 11" form out and associated reader control

Data communications type wheel arrangement with associated four-row keyboard layout (American Standard Code for Information Interchange)

115 V AC 60 cycle synchronous motor unit

Gears for 100 wpm operation (110.0 Bauds)

Adjusted for 72 character line

Horizontal spacing 10 characters per inch

Vertical spacing 3 or 6 lines per inch

Selector magnet driver can accept .020 or .060 amperes with proper wiring (strapping)

Generates "even" vertical parity

Two-tone cover: Ivory and Greige

Copyholder

Answer-back drum to be coded by the customer

Function box "online" operation of line feed, carriage return, bell and WRU

Space suppression at end-of-line

Control key (functions)

Shift key (locks out keys without shift case)

Break key and "Here-is" key

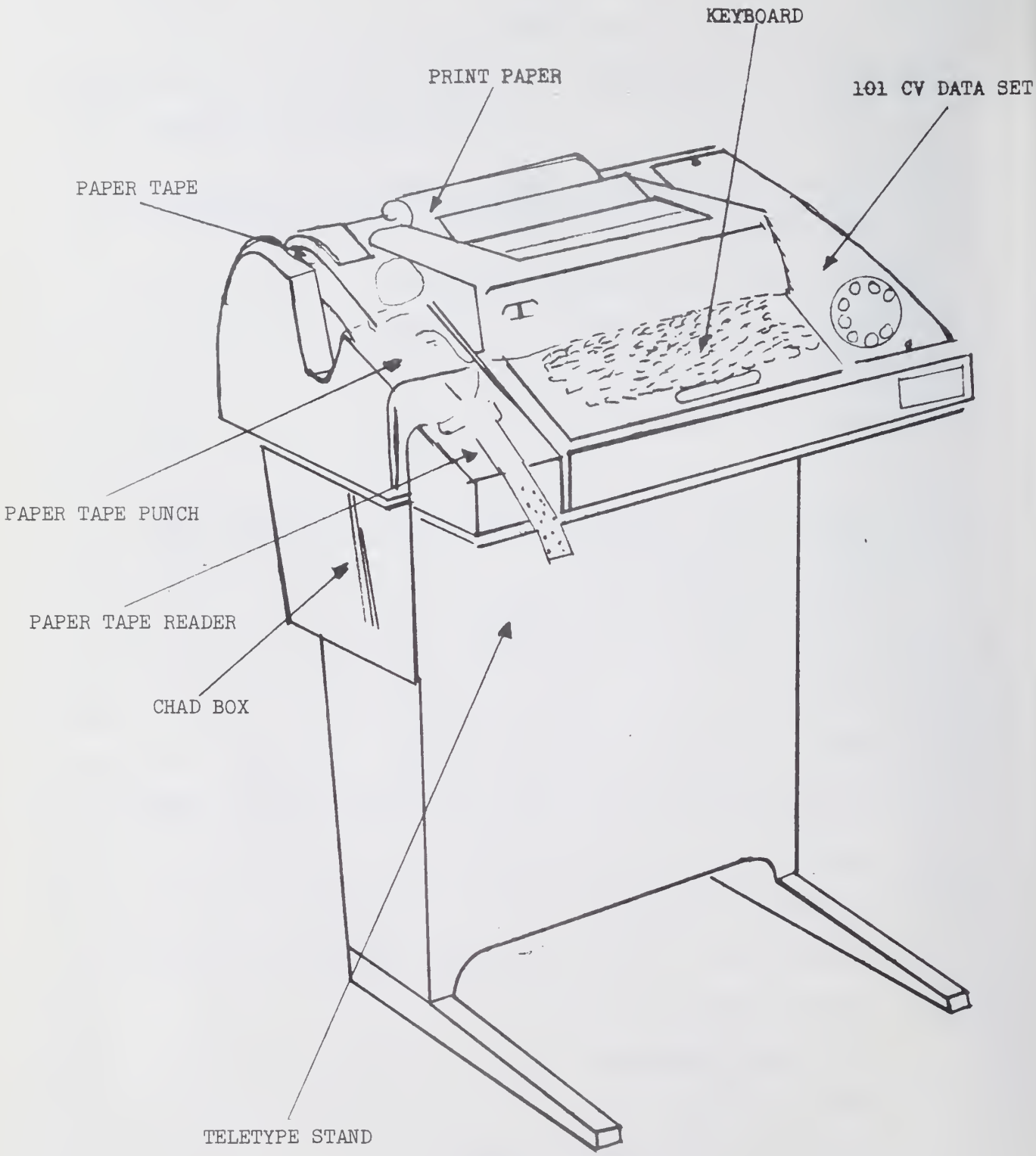
Power supply transformer

Convenience outlet

3-way switch (off, online and local)

Wiring provision for optional full duplex operation

Sheet metal stand with Greige color finish



ASR 33 Teletype

Figure 3

Tape Reader Features

3-way operating switch for start, stop and free position

"End-of-Tape" mechanism to shut down reader

Feed sensing electromagnet is pulsed by the distributor

Automatic control contacts for start and "X-ON" code, stop on "X-OFF" code and low paper alarm

Power pack assembly with automatic control relay

Parallel wire output to distributor

Operating sequence; reads tape and feeds

Capable of reading fully perforated tape

Tape Punch Features

Four operating buttons, "UNLOCK", LOCK "ON", "BACKSPACE", and "RELEASE". (When the lock "ON" button is depressed, the tape punch is locked into the "on" mode and cannot be turned off. When the "UNLOCK" button is depressed, the tape punch will not turn off but will be able to accept an "off" signal and turn off automatically.)

1" Core of tape supply

Fully perforated 8-level code holes and feed holes

"V" shaped tape tearoff

Operating sequence; feed and punch

Removable chad box (designed for attaching to stand)

Automatic control contacts for start on "Tape Aux. On" code, stop of "Tape Aux. Off" code and low paper alarm

General Information

Interoperates with existing teletypewriters having corresponding features

Fewer options possible compared to Model 35 Heavy-Duty Equipment

Actual and schematic wiring diagrams packaged with set

Set shipped completely assembled less stand and chad box

The above equipment requires a channel capable of handling 110.0 Bauds (bits per second) for operation at 100 wpm.

One copy each of Bulletins 273B and 1184B furnished with each

Dimensions

Complete set less stand:

Width	22"
Depth	18-1/2"
Height	8-3/8"
Weight	44 pounds

Stand: Supports Teletypewriter

Width	17-3/4"
Depth (at Top)	8"
Depth (at Bottom)	6-1/2"
Height	22-1/2"
Weight	12 pounds

Estimated Service Life

4500 Hours at 100 wpm

Lubrication Intervals
(Printer, Tape Punch and Reader)

100 wpm	500 hours or 6 months, whichever is first

Preventive Maintenance and Overhaul

100 wpm	1500 and 3000 hours

NOTE: Hours indicates actual operating time.

The Dectapes are connected to the PDP-8 by way of the Data Break Multiplexor feature through a Dectape Control (TC01). The TC01 will be described first.

Control, Dectape TC01

The TC01 Dectape Control operates up to eight TU55 Dectape Transports. Binary information is transferred between the tape and the computer in 12-bit computer words approximately every 133-1/3 microseconds. In writing, the control disassembles 12-bit computer words so that they are written at four successive lines on tape. Transfers between the computer and the control always occur in parallel for a 12-bit word. Data transfers use the PDP-8 Block Transfer Control (BTC) (high speed channel) facility of the computer. As the start and end of each block are detected by the Mark track detection circuits, the control raises a Dectape (DTCF) flag which causes a computer program interrupt. The program interrupt is used by the computer program to determine the block number. When it determines that the forthcoming block is the one selected for a data transfer, it selects the read or write control mode. Each time a word is assembled or Dectape is ready to receive a word from the computer, the control raises a data flag. This flag is connected to the computer facility to signify a break request. Therefore, when each 12-bit computer word is assembled, the data flag causes a transfer via the BTC. By using the Mark channel decoding circuits and the BTC in this manner, computation in the main computer program can continue during tape operations.

Dectape TU55

Dectape is a convenient, low cost in-out data storage facility and updating device.

FIXED POSITION ADDRESSING permits selective updating of tape information as in magnetic disk or drum storage devices. Units as small as a

single computer word may be stored or recorded on tape without disturbing adjacent information. Data blocks are numbered and completely addressable.

AUTOMATIC WORD TRANSFERS use the PDP/8 · Block Transfer Control to allow concurrent information processing and data acquisition during block transfers at 15 kc character rate.

SIMPLE TRANSPORT MECHANISM improves reliability. Dectape's simple drive system requires no capstans, no pressure pad, and no mechanical buffering; therefore tape and head wear is minimal.

POCKET-SIZE REELS are handy to carry, easy to load. Each 3-1/2 inch reel holds up to 3 million bits, the equivalent of 4,000 feet of paper tape, assuming 6-bit words are used.

BI-DIRECTIONAL OPERATION saves time, provides easy access to stored information; reading, writing, and searching may be conducted in either direction.

REDUNDANT, PHASE RECORDING insures transfer reliability, reduces problem of skew in bi-directional operation. Use of phase (rather than amplitude) recording greatly reduces drop-outs due to variations in amplitude.

PRE-RECORDED TIMING AND MARK TRACKS simplify programming. Relieve the programmer of the responsibility of furnishing timing or counting instructions and permit block and word addressability.

PRE-TESTED SUBROUTINES are available for information storage and retrieval, maintenance, and diagnostic tests.

Dectape Transport Type TU55

The TU55 is a bi-directional magnetic-tape transport consisting of a read/write head for recording and playback of information on five channels of the tape. Connections from the read/write head are made directly to the TC01 external control which contains the read and write amplifiers.

The logic circuits of the TU55 control tape movement in either direction over the read/write heads. Tape drive motor control is exercised completely through the use of solid state switching circuits to provide reliable operation. These switching circuits contain silicon controlled rectifiers (SCR) which are controlled by normal DEC diode and transistor logic circuits. The function of these circuits is simply to control the torque of the two motors which transport the tape across the head according to the established function of the device, i.e., go, forward, reverse, or stop. In normal tape movement, full torque is applied to the forward or leading motor and a reduced torque is applied to the reverse or trailing motor to keep proper tension on the tape. Since tape motion is bidirectional, each motor serves as either the leading or trailing drive for the tape, depending upon the forward or reverse control status of the TU55. A positive stop is achieved by an electromagnetic brake mounted on each motor shaft. When a stop command is given, the trailing motor brake latches to stop tape motion. Enough torque is then applied to the leading motor to take up slack in the tape.

Tape movement can be controlled by commands originating in the computer and applied to the TU55 through the TC01 Dectape control, or can be controlled by commands generated by manual operation of rocker type switches located on the front panel of the transport. Manual control is used to mount new reels of tape on the TU55, or as a quick maintenance check for proper operation of the control logic in moving the tape.

PROGRAMMED BUFFERED DISPLAY 338

The Type 338 Programmed Buffered Display is an incremental display system, consisting of a small scale, high speed computer and a display subsystem for control of the CRT. The computer used is the Digital Equipment PDP-8.

FUNCTIONAL DESCRIPTION

The 338 display logic can be thought of as a special purpose computer which stores its instructions (display commands) in the memory of the PDP8, and interacts with the computer through a series of instruction interrupts and data transfers. The display is an output device with respect to the computer for the following reasons:

a. The PDP8 has a series of instructions which start, stop, and load and interrogate the registers of the display.

b. The PDP8 can modify the data commands which are interpreted by the display because the commands are stored in the PDP8 memory.

The commands are transferred to the display control via the PDP8 single cycle data break system. The display file words are loaded into a table or block of successive memory locations; and the beginning location of this table is loaded into a special register called the display address counter (DAC). The output of the DAC and the break field registers are applied to the inputs of the memory (MA) register forming a 15-bit address which can increment across memory field boundaries. The data break is then

initiated by either the display or the computer, and this address is read into the MA. The computer then goes through a break cycle in which it fetches the word from memory and places it into its memory buffer (MB) register from where it is transferred to the buffer register (DX) in the display. During this time, the display starts its operation and the DAC is incrememted by one. The computer program counter (PC) is not incremented during the break cycle. At the end of the break cycle the PDP8 continues its main program until the display requires another data break.

Display Parameters (Coordinate System)

The display screen which is 9-3/8 inches square, has 10 bits of resolution; in other words there are 1,024 points in the x and y directions or about a million points in all. The x and y position registers are 13 bits long, however, and therefore the screen represents only 1/64 the total addressable area (paper). The paper is broken up into 64 sectors corresponding to the upper 3 bits of x and y, with sector 0 defined as the lower left sector. Only information in sector 0 is intensified so that translation is accomplished by moving the paper in relation to sector 0. The lower left corner is point (0,0), and the coordinates increase to the right and up, and decrease to the left and down. An edge violation occurs when a line is drawn across the boundary of the paper. This is a warning that an overflow condition has just occurred in the x or y position register. A vertical edge flag indicates the y position register went from all 1s to all 0s, or from all 0s to all 1s. The horizontal edge flag indicates overflow in the x register. The overflow can be set to occur after the 10th, 11th, 12th or 13th bit in x and y. The virtual size can therefore be changed under program control.

Scale

The scale setting determines the number of positions each succeeding spot is moved before it is intensified. It affects both the size and appearance of lines or symbols drawn in the vector, vector continue, short vector, increment, or character modes. At scale setting 11_2, each point can be clearly distinguished. At scale setting 00_2, lines and symbols appear to be continuous. The point spacing is illustrated in the following table.

Scale	Point Spacing	Intensify
00_2	● ● ● ● ● ● ● ● ● ●	Every
01_2	● ○ ● ○ ● ○ ● ○ ● ○	2nd
10_2	● ○ ○ ○ ● ○ ○ ○ ● ○	4th
11_2	● ○ ○ ○ ○ ○ ○ ○ ● ○	8th

Intensity

There are eight intensity levels available on the display, ranging from 000_2, which is barely visible, to 111_2, which is very bright. Note that scale and intensity settings are interrelated. For example, if characters are drawn (with the character generator) at the lowest scale setting, and too high an intensity is used, they will be badly blurred. On the other hand, if many characters are to be displayed simultaneously or if the light pen is to be used, it is best to use as high an intensity level as possible.

State

The display logic is broken into two states, data state and control state. Control state commands are interpreted as instructions to the display logic to change parameters, jump, skip, etc. The data state commands are instructions to move the beam via the x and y position registers. When the display is initialized, the commands are accepted in control state until an "enter data state" command is given. The display returns to control state from data state by escaping.

In control state, the first three bits (op code) designate the operation to be performed by the remaining nine bits. Seven of the eight op codes are used:

0 Parameter

1 Mode

2 Jump

3 Pop

4 Conditional skip 1

5 Conditional skip 2

6 Miscellaneous (microprogrammed)

- 0 Arithmetic compare 1
- 1 Arithmetic compare 2
- 2 Skip on flags
- 3 Count
- 4-7 Set slaves (optional)

7 Sync

Data state words are accepted in one of seven formats according to the contents of the mode register. The data state modes available are:

Increment Mode - This mode is used to draw alpha numeric characters or other small symbols, and to draw curves. A half-word instruction that will cause the beam position to be stepped one, two, or three times in one of eight directions. Direction 0 is to the right, direction 1 is up and to the right, etc.

Vector Mode - This mode is used to draw straight line segments. A two-word instruction which causes the beam position to be stepped along a line represented by a 10-bit delta y and a 10-bit delta x, each having a sign bit.

Vector Continue Mode - This mode is used to draw a straight line to the edge of the screen. Similar to Vector mode but causes the vector to be extended until an "edge" is encountered.

Short Vector Mode - This mode is used to draw figures composed of short line segments. A one-word instruction having a 4-bit delta y and a 4-bit delta x, plus sign bits. It is transformed within the display to the same format as Vector mode, and operates in the same manner.

The preceding modes are "incrementing;" that is, they move the beam by counting the x and y position registers. The counting is done at 1.2 microseconds per step on an intensified move; at 0.30 microseconds per step on a nonintensified move.

Point Mode - This mode is used for random point plotting. A two-word instruction which causes new y and/or x coordinates to be set into the y and x position registers.

Graph-Plot Mode - This mode is used to draw curves of mathematical functions. A one-word instruction which causes the y or x position register to be changed; at the same time, the other register is incremented by a count of one, two, four, or eight, depending on the current scale factor. This mode is useful for plotting curves resulting from a series of solutions of an equation.

Point and Graph-Plot modes operate at one of two rates, depending upon the position of the new point with respect to the previous point. The high-order three bits of the ten y and ten x position bits are compared to the corresponding bits in the new data words. If they are the same, the delay for beam-settling time is 6 microseconds; if they differ, a 35 microsecond delay is used.

Character Mode - A half-word instruction, using the Type VC38 Character Generator.

All modes are entered from control state by the "enter data state" command. Each mode, however, has its own way of escaping back to control state. The mode register is cleared by power clear and initialization of display (IOT 165).

Subroutining

The display has control state commands which will modify the DAC. This enables unconditional display jumps (jump), jump to subroutine (push jump) and the return from subroutines (pop). The new address is specified by 15 bits allowing direct addressing of 32 K of core. The jump and push

jump commands are specified by two consecutive 12-bit words. Push jump stores the return address, mode, intensity, scale, and light pen on a push-down pointer list which resides in the first 4 K of PDP8 core. This information is automatically written into two locations in the format shown below.

Break Field			Light Pen	Scale		Mode			Intensity		
0	1	2	3	4	5	6	7	8	9	10	11

First Word

Low Order 12-Bits of Memory Address											
0	1	2	3	4	5	6	7	8	9	10	11

Second Word

The information is placed in the address indicated by the push-down pointer, (PDP) which is a 12-bit register in the display logic. When a push jump is executed, the PDP is incremented twice, adding a new entry to the PDP list. This allows multi-level and recursive subroutines in the display.

The pop command takes the last entry on the PDP list from core and gates it back to the proper registers. The display status, however, can be inhibited from being restored. The PDP is automatically decremented by two, making the PDP list a last in first out stack.

Light Pen

The light pen is an input device which generates a signal (flag) that can be sensed and interpreted by the computer. A light pen interruption stops the display, leaving the contents of all display registers intact, and signals the computer that an interruption has occurred. When this happens, the programmer can examine the contents of the display registers to determine the location (on the display) of the point of light that was sensed by the light pen and/or determine the memory location of the data word specifying that point. The light pen detects light in the range 4300 to 5600 angstroms.

Pushbuttons

The 338 is equipped with a bank of twelve pushbuttons. They are placed six in a row with a clear button to reset that group. The buttons in each group are interlocked, but two buttons in different groups can be pressed simultaneously. Pressing a button complements an associated flip-flop. For reference, the pushbutton is lit when its flip-flop is in the 1 state. The state of the pushbuttons can be sensed both by the display, using the control state skip instructions, and the PDP8, which can read the state of the pushbuttons into the accumulator. The PDP8 and display can also clear and set the pushbuttons. This enables three-way communication between the operator, display logic, and PDP8. The buttons are labeled 0 through 11 and are packaged in a compact, portable box. The box is connected to the display by a 20 foot cable. There is also a special computer interrupt button on the box.

Flags

There are a number of special conditions that can arise in the display which require the attention of the PDP8 processor. These conditions are indicated by display flags which can interrupt the computer and be sensed by IOT skip instructions. The flags are:

a. Internal stop

b. External stop

c. Edge

d. Light pen find

e. Push button hit

f. Manual interrupt

The flags can be separated into two groups; a-d are flags which stop the display; e-f are flags which do not stop the display. Group 1 flags are cleared in one of three ways: initialization of a display sequence; resuming from the point the display stopped; and a pulse to clear the flag if the display is no longer needed.

Interval Timer

The basic system was installed with an interval timer. It was changed to synchronize with the line voltage. The orders associated with the timer are:

6311 Skip on no timer flag,

6312 Clear timer flag, enable timer interrupt,

6314 Disable timer interrupt.

(H. Levin)

Operating Additions

Very soon after the Graphics 8 was put into operation it became obvious that it could not stand alone and was in need of a number of hardware improvements. The list began with a slow link to a large 360 installation and carried through a Data Disc for more local storage, a Data Tablet for input, an Audio Output for sound production, a push button bootstrap for convenience, an Illiac III connection for testing applications, a 2701 P.D.A. for more rapid access to 360 and a microswitch keyboard for replacement of the teletype keyboard.

PDP8 TO 630 INTERFACE

General Description

The PDP8 to 630 interface is a half duplex, 100 CPS, serial input to the 630 Data Communications unit. The 630 has no knowledge of the port being anything other than a high speed serial device.

The interface consists primarily of:

1. An entry to the PDP8 accumulator,
2. An entry from the PDP8 accumulator,
3. Six IOT instructions to control transfers,
4. An entry to the PDP8 skip bus, interrupt bus, and clear ACC bus,
5. A DEC 4706 receiver card, and 4707 transmitter card,
6. Miscellaneous control logic.

Instruction Set

IOT 6631 - SKIP ON RECEIVER FLAG
6632 - CLR ACC AND REC FLAG
6634 - GATE REC TO ACC

6641 - CLR INT. ENABLE
6642 - SET INT. ENABLE
6644 - CLR TRANSMITTER FLAG AND INPUT DATA FROM ACC

Due to the half duplex mode of operation an echo is generated in the receiver when data is transmitted. This allows testing of transmitter completion with an IOT 6631.

Transmitter

Transmitting data to the 630 consists of gating the ACC. contents into the transmitter with an IOT 6644. The interrupt enable

flag must have been set with an IOT 6642 in order to test for transmitter completion. The IOT 6644 also enables the shift clock and starts transmitting data. The receiver is active during transmission and receives the transmitted data as it is going to the 630. When the receiver flag comes on, it has received the complete character. A test of the receiver flag with an IOT 6631 will generate a program skip when the flag is present. A new character may then be transferred from the accumulator to the transmitter.

Receiving

Receiving data from the 630 consists of clearing the receiver flag and enabling the interrupt. An incoming character will set the receiver flag and generate an interrupt (if allowed). A test of the receiver flag with an IOT 6631 will generate a program skip, indicating a character is present. An IOT 6634 will gate the contents of the receiver into the accumulator.

(R. Miller)

Data Disk

The following information describes our disk storage system with the exception that:

The 64 heads of electronics will be divided into 32 groups of 2 heads each.

Summary of Specifications

Disk Speed	1800 RPM +1.32 - 3% Hysteresis Synchronous Motor
Data Rate	3.0 Mbps per track
Data Capacity	100,000 bits per track (tracks can be added in increments of 8, up to 64.
Input/Output Levels	0 and +5V TTL integrated circuit interface
Environmental	Operating temp: 50°F. - 105°F.; less than 20°F. change per hour.
	Non-operating: -20°F. - +130°F.
	Operating humidity: 10% - 80% RH without condensation.
	Non-operating humidity: to 90% RH without condensation.
	Corrosive atmospheres such as those found in steel and chemical plants are not permitted.
	Floor vibration of 0.15 g's max. from 10 to 65 Hz.
	The disk package shall not be damaged by 5 g's or less of shock in any axis.
AC Power	120V ± 10%, 60 Hz +0.5 -1.5 Hz single phase 8.2A starting (10 sec.); 2.6A running
DC Power Requirements (Per track)	+18V at 125 ma (while writing) +6V at 90 ma) -6V at 40 ma) ±5% regulation

(Power supplied by internal power supply.)

Weight	86 pounds

General Description

Electrical

The F-series Parallel Digital Disk Memory System has a 12-inch disk which can contain as many as 64 data tracks with 100,000 bits on each track. The disk rotates at 1800 RPM and the bit rate is 3 million bits per second.

The FPD unit is designed for display buffer storage applications. The disk unit uses synchronous clocking from a clock track and is recommended for temporary storage only. Where data is to be stored for an indefinite period, the Data Disk F6 Memory should be employed.

Each track is complete with a read/write head and all electronics to perform the following functions (Figures 4, 5):

Encode data
Write data
Read data
Decode data
Re-clock data

Any number of tracks may be written or read in parallel, since each has a clocked flip-flop output.

System Application

The FPD unit is designed so that each track on the disk may feed a separate TV monitor display. A high-speed processor can access each track and update the presentation stored upon any track. Where display rates higher than 3 million bits per second are needed, more than one track can be combined to form the display buffer. For example, data read from four channels may be loaded into a four-bit shift register and with a 4X clock the data can be shifted into the display channel at a 12 million bit rate (Figure 6). Any number of tracks, up to 64, may be combined.

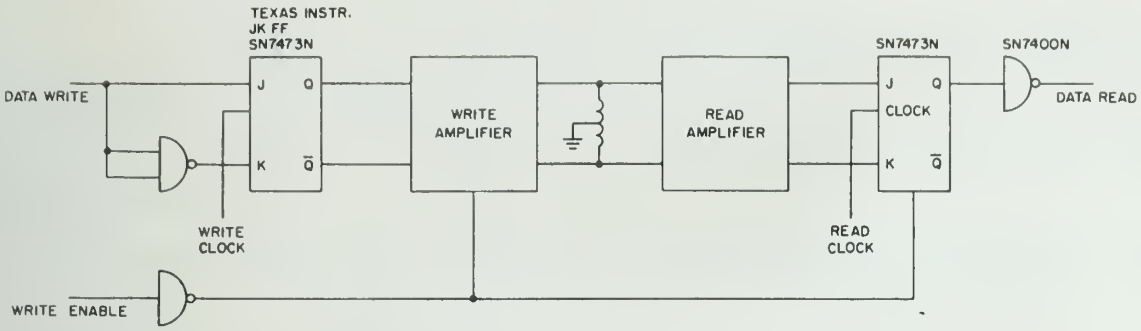


Figure 4

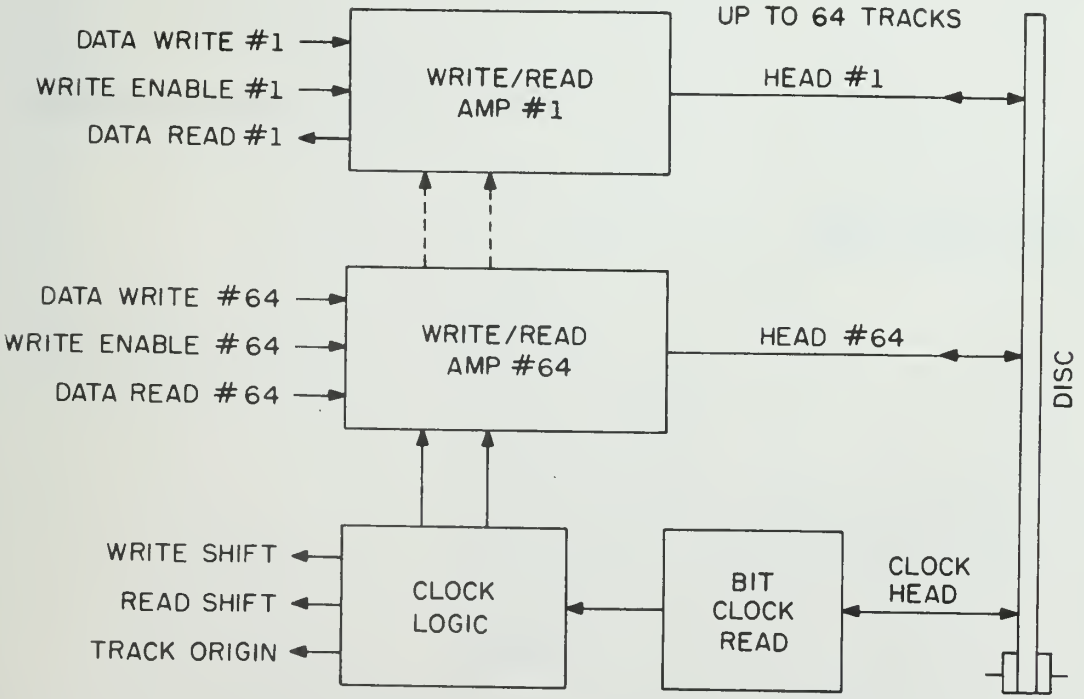


Figure 5

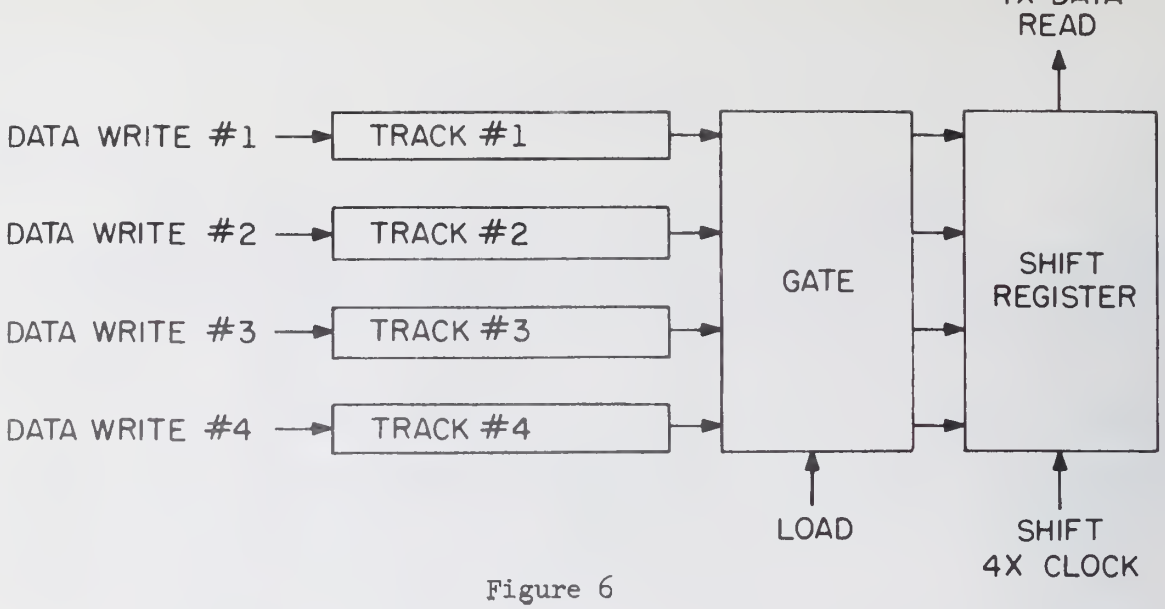


Figure 6

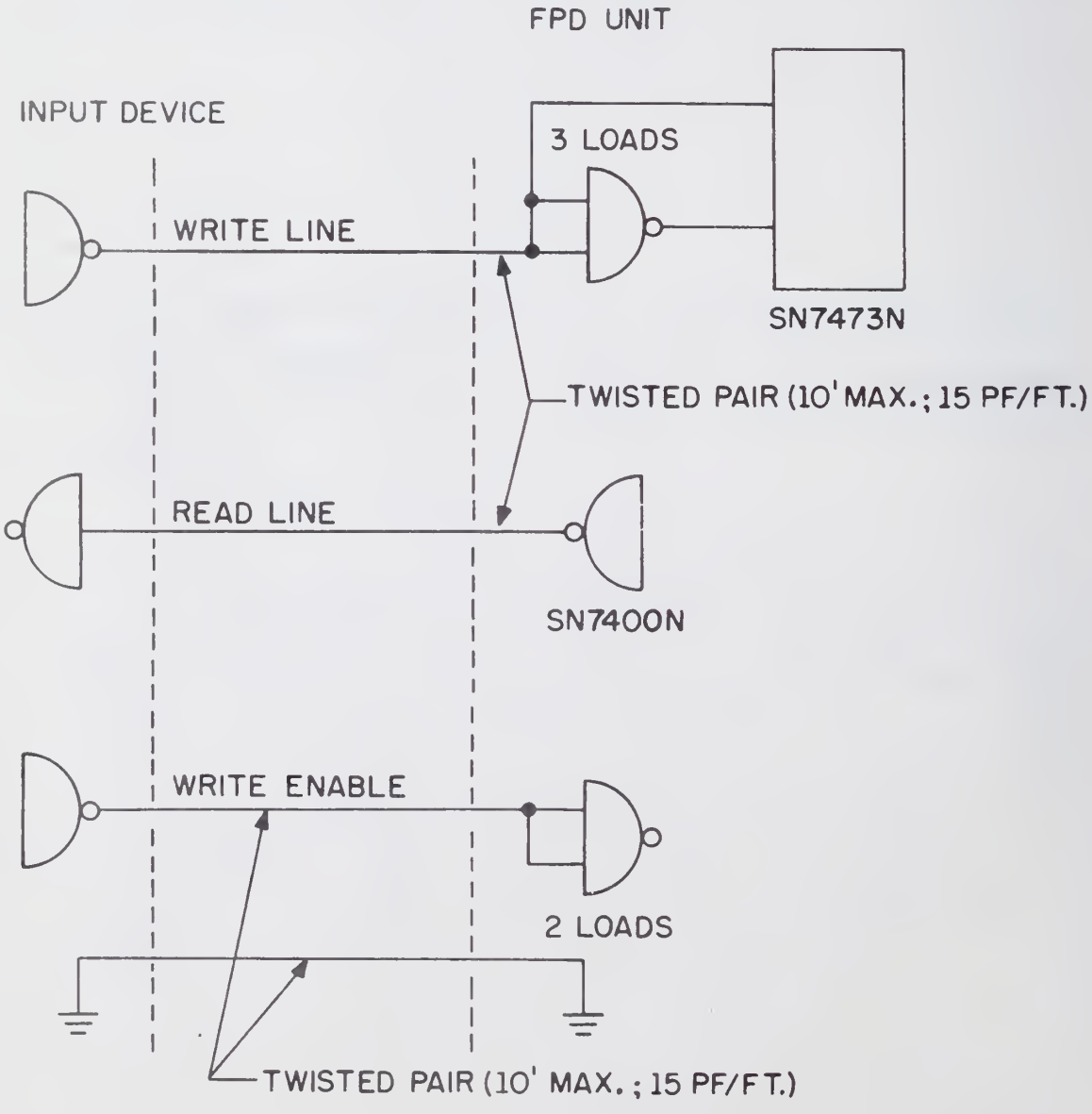


Figure 7

Input/Output Lines

Each track has three input/output lines that are sent over two twisted pairs of cables, as shown in Figure 7. The FPD unit uses Texas Instrument Series SN7400N and SN7473N TTL integrated circuits.

Input Connectors

Eight 34-pin connectors are provided, each serving eight heads. The use of 16 heads would require two connectors, etc. All eight connectors (S1 through S8) would be required if 64 heads were used. (See Table 2.) Table 2 also indicates the function served by each pin on each connector, as well as the tracks served by each.

Table 1

Data Input/Output Lines

Data Write 1 thru 64:	An input line that is driven from output of a flip-flop that is clocked by Data Write Shift Clock.
Write Enable 1 thru 64:	The Write Enable line going high will cause the data on the corresponding Data Write line to be written on the track. As long as the Write Enable line is high, writing will continue.
Data Read 1 thru 64:	Each Data Read line is the buffered output of a clocked flip-flop. The Data Read is delayed 2 bits times from Data Write and may be shifted into an external register by using the negative edge of Data Read Shift Clocks. During Write the output of the Data Read line is held low.

Pin No.	Function	Tracks Assigned to Conn. S1 S2 S3 S4 S5 S6 S7 S8	Pin No.	Function	Tracks Assigned to Conn. S1 S2 S3 S4 S5 S6 S7 S8
A B	*Data Write Track No. Data Read Track No.	1 9 17 25 33 41 49 57 1 9 17 25 33 41 49 57	U V	*Write Enable Track No. *Ground	1 9 17 25 33 41 49 57 1 9 17 25 33 41 49 57
C D	*Data Write Track No. Data Read Track No.	2 10 18 26 34 42 50 58 2 10 18 26 34 42 50 58	W X	*Write Enable Track No. Ground	2 10 18 26 34 42 50 58 2 10 18 26 34 42 50 58
E F	*Data Write Track No. Data Read Track No.	3 11 19 27 35 43 51 59 3 11 19 27 35 43 51 59	Y Z	*Write Enable Track No. Ground	3 11 19 27 35 43 51 59 3 11 19 27 35 43 51 59
H J	*Data Write Track No. Data Read Track No.	4 12 20 28 36 44 52 60 4 12 20 28 36 44 52 60	a b	*Write Enable Track No. Ground	4 12 20 28 36 44 52 60 4 12 20 28 36 44 52 60
K L	*Data Write Track No. Data Read Track No.	5 13 21 29 37 45 53 61 5 13 21 29 37 45 53 61	c d	*Write Enable Track No. Ground	5 13 21 29 37 45 53 61 5 13 21 29 37 45 53 61
M N	*Data Write Track No. Data Read Track No.	6 14 22 30 38 46 54 62 6 14 22 30 38 46 54 62	f g	*Write Enable Track No. Ground	6 14 22 30 38 46 54 62 6 14 22 30 38 46 54 62
P R	*Data Write Track No. Data Read Track No.	7 15 23 31 39 47 55 63 7 15 23 31 39 47 55 63	h i	*Write Enable Track No. Ground	7 15 23 31 39 47 55 63 7 15 23 31 39 47 55 63
S T	*Data Write Track No. Data Read Track No.	8 16 24 32 40 48 56 64 8 16 24 32 40 48 56 64	j k	*Write Enable Track No. Ground	8 16 24 32 40 48 56 64 8 16 24 32 40 48 56 64
m	Unassigned		n	Unassigned	

Table 2

Clocks

Five clocks, all derived from one track, are available in the standard FPD system. Two are used internally, and the other three are for use at the interface. The three interface clocks are the Track Origin (once per revolution), Write Shift and Read Shift (Figure 8 and Table 3).

The Write Shift Clocks are used to change the state of the Data Write line and are counted down to indicate angular position of the disc. The Track Origin clock is derived from the six-bit gap in the clock track and is used to indicate the zero degree position of the disc and as a reset for any counters used to identify other angular positions.

Clock Connector S9

S9 is a 34-pin used by the clock track only. (See Table 4 for pin assignments.)

Table 3

Clock Output Lines

Data Write Shift Clock:	A 3-million bit per second clock with 6 clocks missing at Track Origin time. The negative edge is used for changing state of Data Write lines.
Data Read Shift Clocks:	Inverted Data Write Shift Clocks. The negative edge is used for sampling the Data Read lines. The Data Read is delayed 2 bit times from Data Write.
Data Origin Clock:	A once-per-revolution clock used to reset counters, etc.

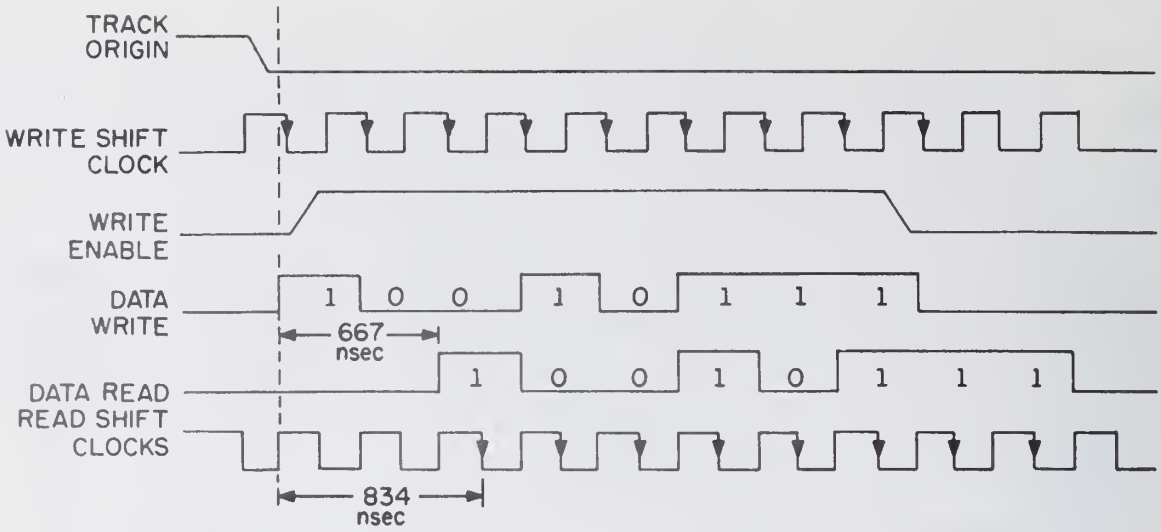


Figure 8

Table 4

Pin Assignment
34-Pin Clock Connector S9*

Pin No.	Function	
A B	Write shift clocks) Ground)	Twisted pair
C D	Read shift clock) Ground)	Twisted pair
E F	Track origin clock) Ground)	Twisted pair
H J	Clock data write line) Clock write enable line)	Twisted pair

*Data Disc No. 2535
Winchester MRAC 34P

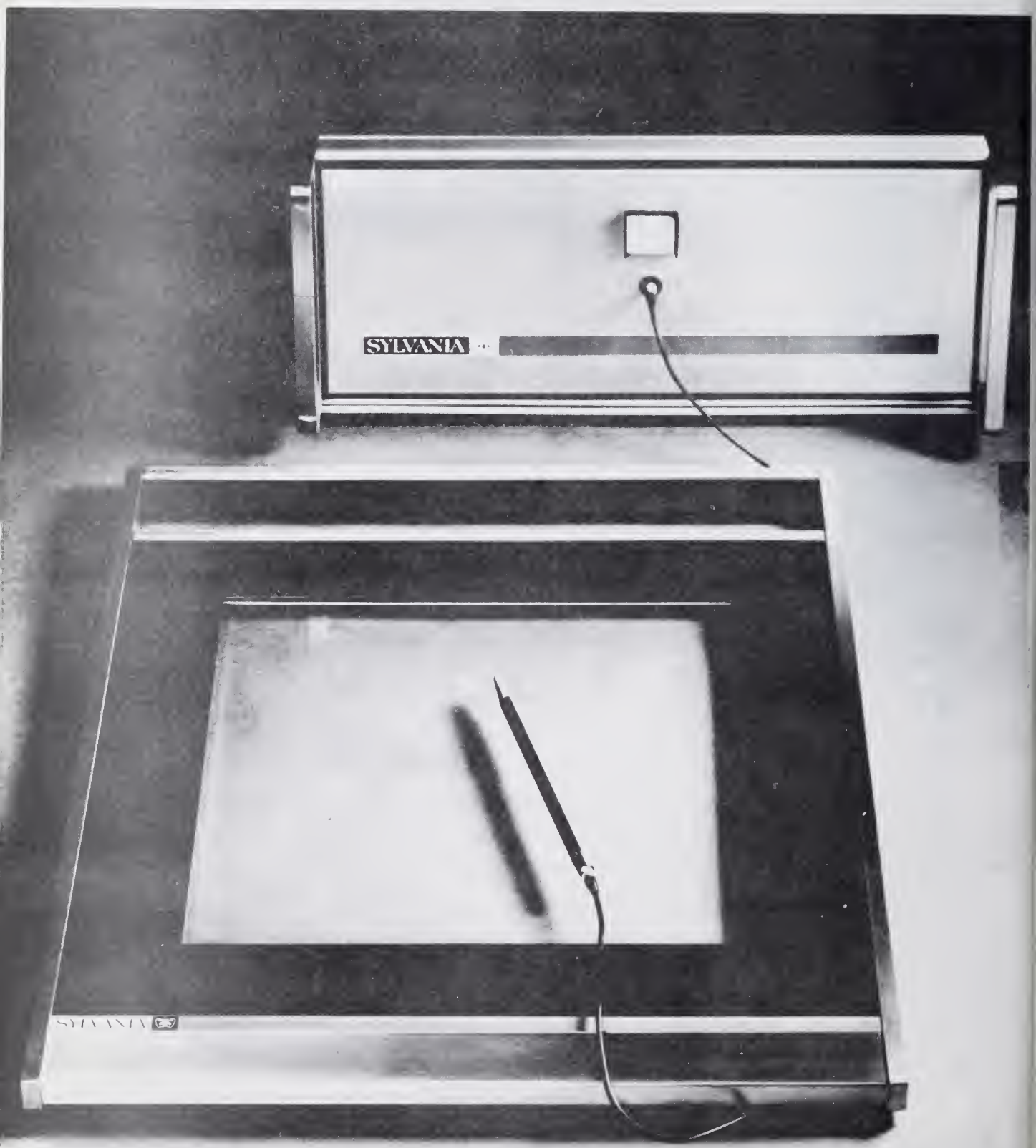
Operation

Write

To write, the first bit of data is placed on the Data Write line and at the correct angular position the Write Enable line is raised and writing begins. Each negative-going transition of the Write Shift clock is used by the external device to transfer another data bit onto the Data Write line. The turn on of the Write Enable should occur at no later than 100 nanoseconds of the negative edge of a Write Shift clock. Write Enable should be turned off at the next positive-going clock transition following the last shift clock. (See timing diagram, Figure 8.)

Read

During Write the Data Read line is held low but at all other times, any data on the track will be clocked out to the Data Read line. The data may be transferred from the Data Read line to an external device at the negative edge of the Read Shift Clock.


SYLVANIA

SYLVANIA DATA TABLET

GENERAL INFORMATION

Introduction

The SYLVANIA DATA TABLET MODEL DT-1 is a coordinate encoder designed to permit graphical communication between man and computer. This solid state system enables the user to enter hand-printed alphanumeric data, curve tracing and modification data, or any other form of hand-generated graphic data into a computer system. The DT-1 is completely contained within three units--a metal rimmed transparent glass writing panel, an electronic pen, and a 1.5 cubic foot electronics package.

Description

The Sylvania Data Tablet is inherently an analog device in which coordinate information is obtained by phase measurements. Several advantages are forthcoming from this: First, the continuous nature of analog signals allows infinite resolution limited only by system noise. Second, since amplitude stability is not necessary, a capacitance pick up (pen) can be used and dielectric layers may be interposed between it and the active surface. The writing panel of the Sylvania Data Tablet consists of a transparent, continuous conductive film bonded to a heavy glass base plate. A thin glass sheet is laminated to the exposed surface of the film to prevent wear and contamination. A drive network coupled to the electronics package excites the film at discrete points along its circumference in such a manner that a traveling wave (in a mathematical sense) is established parallel to each orthogonal axis. This wave has the property that its phase is a linear function of position as in the relationship:

$$V = K \sin (\omega t - \alpha \chi)$$

The actual tablet signals are more complicated due to the requirement for axis separation. The latter is accomplished by introducting individual frequency translations to the drive signals.

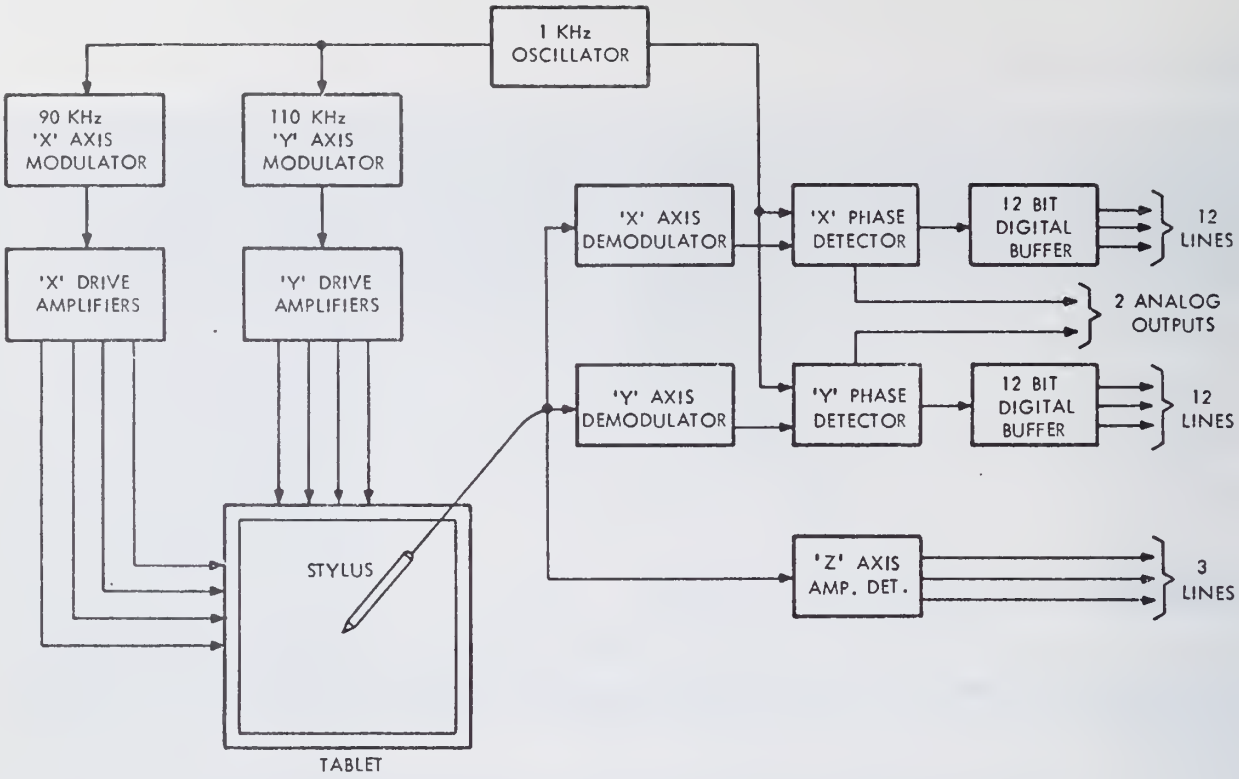


Figure 9 Sylvania Model DT-1 Block Diagram

Figure 9 is a block diagram of the Sylvania Data Tablet. A stable 1 KHz sinusoid oscillator generates the primary signal (which will later contain the desired phase shift) used in the system. Balanced modulators operating with 90 KHz and 110 KHz carrier frequencies multiplex the primary signal to different portions of the frequency spectrum as double-sideband suppressed-carrier signals. These are buffered by the 'X' and 'Y' drive amplifiers which in turn drive the conductive film network through a shielded drive cable. An electronic pen (with a high input impedance amplifier built in), capacitively senses the field in the region beneath the pen tip through the glass laminate and any overlayed paper. The voltage is transferred to the electronic package via the attached coaxial cable.

Circuitry within the electronics package separates the pen signals into 'X' and 'Y' channels and extracts the phase information. The desired phase is observed in the envelope waveform of the signals while the axis information is contained in the carrier frequencies. 'X' and 'Y' axis demodulators, which are in fact synchronous detectors keyed by the carrier oscillators, extract the 1 KHz envelopes from the complex pen signals. Phase detectors then compare the demodulator outputs against the 1 KHz primary signal and produce analog and digital voltages proportional to the phase shifts.

An additional circuit measures the amplitude of the pen signals and provides a coarse measure of height ('Z' axis).

Specifications

SYLVANIA DATA TABLET MODEL DT-1

ELECTRICAL

Accuracy	± 1% of full scale in each coordinate axis
Resolution	± .025% of full scale or 12 binary bits at 5 Hz bandwidth
Bandwidth	20 Hz supplied
Data rate	200 coordinate points per second
Digital outputs:	
'X' and 'Y' axis	Two 12 bit buffer register outputs available--updated every 5 milliseconds
'Z' axis	One bit for each threshold. Output levels are designated 000, 001, 011, 111--updated independent of system timing.
Data Ready Line	Set to 'zero' five microsec. before X-Y buffers change and reset to 'one' state five microsec. after change
'One' state	+4 volts
'Zero' state	+.5 volts
Maximum load	600 pf. at 10 milliamps for either state

Analog Outputs:

'X' and 'Y' axis	Two buffered output lines with a dc voltage proportional to position. Range is from -2 volts to +2 volts with zero at the center. Output impedence is 500 ohms.
'Z' axis	Same as digital except inverted. Output impedance is 850 ohms in high state and 20 ohms in the low state.

External connectors and controls:

Front panel	Power on-off switch with built-in pilot light.
	Miniature coaxial connector for the electronic pen
	14 pin auxiliary writing panel connector
Rear panel	34 pin digital output connector containing the 'one' side of the 'X-Y' buffer registers. Three 'Z' axis bits and the Data Ready Line are also available.
	9 pin analog output connector containing 'X' and 'Y' dc outputs and three 'Z' axis bits.
	14 pin writing panel drive connector
	Three-prong power connector
	Power line fuse--3 amps
	Three power supply fuses--3 amps
Power source	105 to 125 volts 60 Hz, 150 watts
Operating temp. range	+10°C. to +40°C.

MECHANICAL

Writing panel dimensions	15" x 16" x 3/4"
Writing aperture	11" x 11"

Electronic package dimensions	17" x 18 1/2" x 7"
Writing panel weight	Approximately 15 pounds
Electronic package weight	Approximately 35 pounds
Pen replacement cartridge	"Papermate" standard refill

Operation

The Sylvania Data Tablet Model DT-1 may be used as a table-top unit or a transparent overlay for a computer-controlled cathode ray tube display. For the latter use, the bottom plate must be removed by taking out the eight mounting bolts on the bottom. The writing panel may then be mounted over the face of the CRT and the electronic pen used in a "light pen" fashion. Rear projection techniques may also be employed by placing a translucent diffusing overlay on the writing panel.

The electronic package may be converted from table top to relay rack operation by attaching the included adaptor brackets. The writing panel may be mounted up to ten feet (with appropriate cable) from the electronic package using either the front or rear 14-pin panel connectors. The electronic pen can only be connected at the front panel of the electronic package. Analog outputs are available on a 9-pin jack and digital outputs on a 34 pin jack both mounted on the rear panel. A three prong connector and power cord are supplied for connecting 115 volts, 60 Hz to the Model DT-1.

The digital output is a binary parallel format for the 'X' and 'Y' axis. Two 12-bit words are simultaneously stored in buffer registers which are updated 200 times per second by internal timing signals. A Data Ready Line, available at the digital connector, drops to the "zero" state five microseconds before the buffer registers are updated and returns to the "one" state five microseconds following the transfer. Only 100 nanoseconds are required to load the buffer registers which remain quiescent during the

remainder of the five millisecond period. The center of the tablet corresponds to binary 100 000 000 000. The left and bottom edges are represented by 000 000 000 000; the top and righthand edges by 111 111 111 111.

A 'Z' axis (pen height above the writing panel) three-bit word is also available at the digital connector. Each bit corresponds to an adjustable threshold level and is independent of digital timing. As the stylus approaches the writing panel surface from a remote position, the 'Z' representation changes in the following manner: 000 (over 1 inch away), 001, 011, (touching the tablet), and finally 111. The maximum value is reached only when a slight downward pressure is applied to the pen forcing the closure of built-in switch contacts.

The analog outputs are internally buffered and are protected against short circuit. Zero volts corresponds to the center position while the left and bottom edges produce minus two volts dc; the right and top edges produce plus two volts dc. Both analog outputs and three 'Z' axis bits are available on the 9-pin analog connector.

PDP/8 MUSIC GENERATOR

Introduction

The PDP/8 music generator is a low cost device that is capable of producing audio tones over a speaker. Its main purpose is to allow a program to audibly signal a user about various conditions, e.g., an illegal command has been entered, an error has occurred, etc.

Hardware

The music generator consists of:

1. An IOT decoder board;
2. Two flip-flops resistively coupled to:
3. An audio amplifier;
4. A loudspeaker.

Instructions

The following instructions are used in programming the music generator:

67Ø1 - clear both flip-flops

67Ø2 - complement flip-flop 1

67Ø4 - complement flip-flop 2

PDP/8 BOOTSTRAP LOADER--

HISTORY AND GENERAL DESCRIPTION

The PDP/8 bootstrap loader was designed to do away with two very messy and time consuming features of the PDP/8.

The PDP/8 rim loader formerly had to be toggled in by hand, using the accumulator switches. This consisted of toggling in 16 instructions and depositing them in core memory. This loader is necessary to read paper tape.

The PDP/8 tape loader (20 instructions) was formerly read in via the teletype 10 CPS reader. The rim loader must have been present in order to activate the reader. The tape loader is necessary in order to use the Dectapes.

The bootstrap loader allows one to select either the rim or the tape loader option via a switch. The starting address of the selected bootstrap -1 must be set into the acc. switches and loaded with the load address key. The acc. switches are then cleared to all o's and the loader pushbutton depressed. The selected loader is automatically loaded into the PDP/8 memory. The teletype reader or the Dectapes are then ready to use.

The accumulator entry is made to the unused side of the accumulator switches. The set line is the deposit switch.

Logic Description

The loader uses a gated clock for timing and a flip-flop register for decoding. The decoder register length is selected by the

bootstrap selector switch. The selector switch also gates the outputs of two diode matrix boards to the accumulator. Either one or the other of the two matrix boards is connected to the accumulator entry.

When the pushbutton is depressed, the clock is enabled and counts the decoder register to output the first word into the accumulator. The clock output is also used to set the deposit switch entry on the PDP/8. At clock frequency, the decoder outputs consecutively gate words from the selected matrix to the accumulator entry and the deposit line is switched. At the proper count for the selected matrix, the clock is disabled and further action is inhibited until the pushbutton is released and depressed again.

Setting the starting address to -1, when loading the loader, is necessary to insure the output of the matrix in a static condition is all o's. This will not interfere with the normal use of the accumulator switches.

ILLIAC III INTERFACE

The interface from the PDP/8 to Illiac III is an accumulator interface. It has the capability of transferring information to and from the PDP/8 accumulator. The interface has an entry to the PDP/8 program skip bus and several IOT instructions to control the transfer. There are two control flops to control the status of the interface at the PDP/8 END, device ready, and data ready.

IOT List

6731 - SKIP ON DEVICE READY

6732 - CLEAR DEVICE READY

6734 - CLEAR DATA RDY

6741 - SKIP ON DATA RDY

6742 - GATE ACCUMULATOR, SENT TO ILLIAC 3 AS DATA ACCEPTED

6744 - SENT TO ILLIAC 3 AS CONTROL

6751, 6752, 6754 } SENT TO ILLIAC 3 AS CONTROL

2701 PARALLEL DATA ADAPTER*

In order to improve the communications capability to the 360 computers in the Department, a better hardware link was required. The IBM 2701 parallel data adapter was chosen for interface purposes for at least the following reasons.

1. The 2701 allows the PDP/8 to be reasonably well isolated from the 360 channels. Thus, less chance of a system interference.

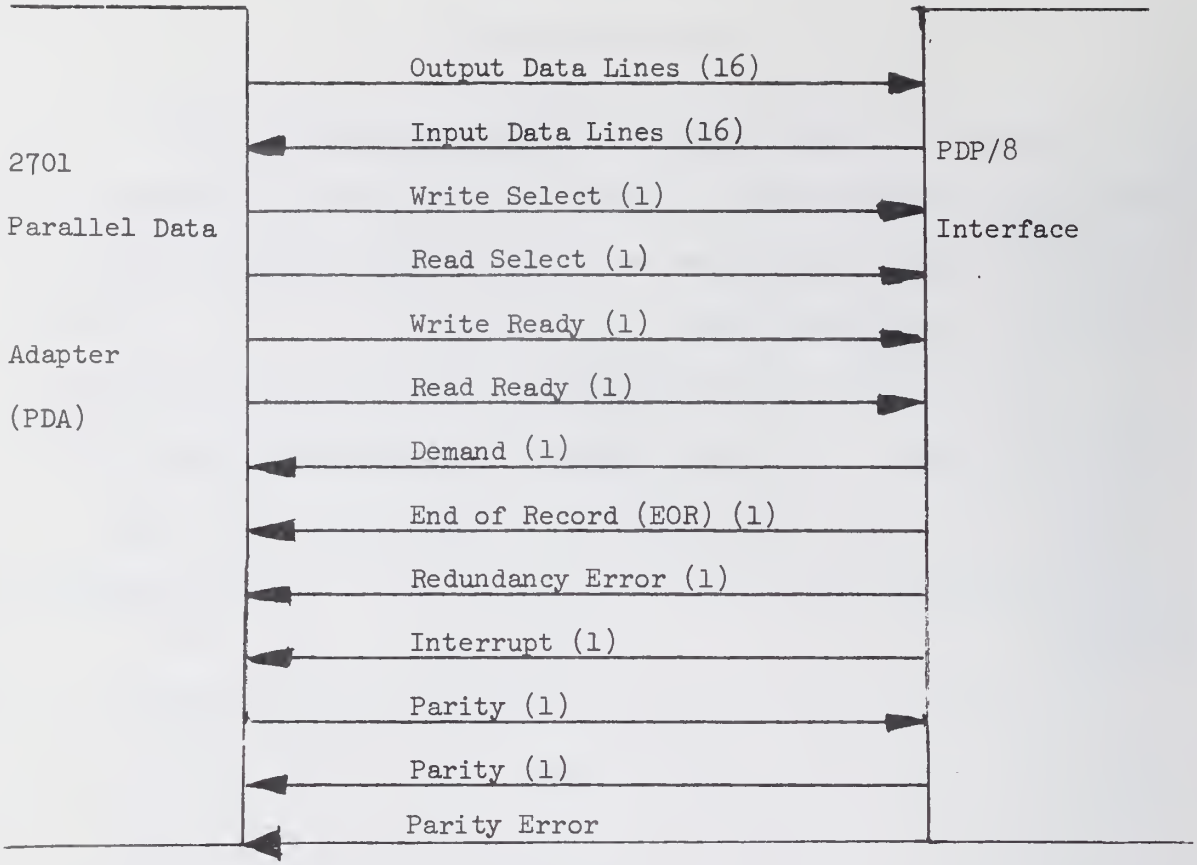
2. The parallel data adapter is a much simpler control that operates in a parallel-by-word (16 bits)-fashion over a demand-response interface.

3. This type of interface had been done before for a PDP/7 so there was some familiarity with its design.

The general operating characteristics of the PDP/8-2701 PDA interface is such as to allow either computer (360 or PDP/8) to initiate a block transfer. The 16 bit word that is transferred to the 360 is broken into two bytes of 8 bits each for 360 channel transfers. The 16 bit word as it arrives at the PDP/8 is broken into two 6 bit characters. The other four bits are not used.

The hardware requirement for this interface was to construct a controller that would exchange information with the PDP/8 data break facility on one side and the 2701 PDA on the other. The data break requirements are reasonably simple to satisfy. The 2701 PDA interface requirements are given below.

* See Report No. 372 for more detail.



OUTPUT DATA LINES. From the PDA to the interface buffer register. While the word is held in the buffer register, parity is generated in the interface and compared with PDA parity.

INPUT DATA LINES. From the interface buffer register to the PDA. Parity is generated in the interface and sent to the PDA.

WRITE SELECT. From the PDA to the interface to signal a write operation from the 2701. This line also generates an interrupt to the PDP/8 if the write enable flop is set.

READ SELECT. From the PDA to the interface to signal a read operation from the 2701. This line also generates an interrupt to the PDP/8 if the read enable flop is set.

WRITE READY. From the PDA to the interface. This line notifies the interface of a data word on the bus. The data is valid and settled before the line is raised.

READ READY. From the PDA to the interface. This line notifies the interface it is available and ready to accept a word from the bus.

DEMAND. To the PDA from interface.

WRITE COMMAND. Signifies the interface has accepted the word on the bus.

READ COMMAND. Signifies the data on the bus is valid. Read data must be valid for the duration of the demand signal.

REDUNDANCY ERROR. (Interface Parity Error). Interface to PDA. Indicates the interface has detected a parity error on a write operation.

END OF RECORD (EOR). Interface to PDA. This line signifies the interface has completed the operation and will not generate or accept any more data. This line also causes the PDA to present device end and channel end status to the 360 channel.

INTERRUPT. Interface to PDA. Signals the PDA to interrupt the CPU through the channel.

PARITY. PDA to interface. Parity is sent simultaneously with the data bus. The interface gates the data bus into the buffer register, and calculates parity to be compared with the PDA parity.

PARITY-INTERFACE TO PDA. The interface buffer register is loaded from the P.D.P.8 and parity is calculated from the register contents. The data and parity is sent simultaneously to the PDA.

PARITY ERROR The 2701 PDA signals the PDP/8 when an error is detected when checking parity on a read operation.

More detailed information can be found in the Department of Computer Science Report #323 titled "DEC PDP/8 Interface to IBM 2701 PDA."

Microswitch Keyboard (see figures 10, 11)

The microswitch keyboard is an assembly of switch modules into a standard array of keys for alphanumeric character entry. Our particular keyboard is ASCII codes so as to be somewhat compatable with our other teletype keyboards.

The features of this keyboard that influenced our choice were (1) the integrated ckt. compatability, (2) the single power supply requirement, (3) the Hall Effect switch. The integrated ckt. compatability saves a lot of level conversions and logic changes when applying the keyboard. to hardware interfaces. The single power supply requirement certainly makes life simple when using the keyboard with other devices. The Hall Effect switch should allow the operation to be quiet and reliable.

Switch Specifications

Power Requirements	5V. DC. ±5%
Current Drain	Standby: 15 MA/switch
Output Capacity	Quiescent: 100 μA leakage
	Operated: 3.5V @ 10MA
Temp. Range	Operating: +35° to +125°F
	Non operating: -40° to 160°F R.H. 95%
Force at Operating Point	3 oz. nominal
Pretravel	0.125 in. (+0.025 -0.050)
Total Travel	0.187 in. nominal
Release Point	0.40 in. min. from free position

Figure 10

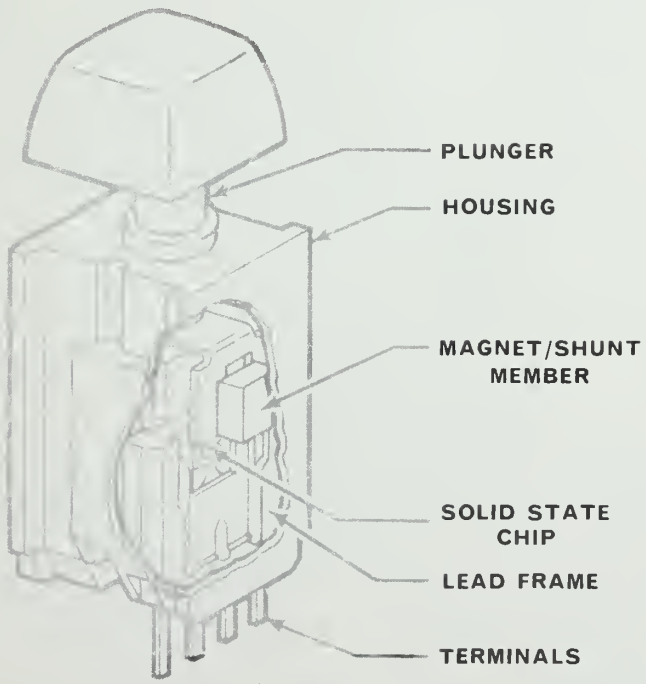


Figure 11

PROPOSED ADDITIONS

As the general capabilities of the graphic system have increased through its software development, communications interfaces and hardware additions it has become more apparent that two things were needed for applications. These were (1) a more rapid means of local printout and (2) more terminals for simultaneous graphic operations.

After some looking, the Teletype Inktronic printer was chosen for the printout. The main reasons for this choice were (1) price ($5300) and (2) almost no mechanics. The speed of 2 lines/second with no mechanical carriage return was appealing for our PDP8. The prospects of having a printer that was completely Electronic was likewise appealing from the maintenance point of view. A description of the Inktronic is given in this section.

The method we chose for getting more terminals is described under the heading of Display Processing Unit. It was taken directly from DCS Report No. 343.

INTRONIC PAGE PRINTER

GENERAL

The receive-only "INKTRONIC" system forms characters from a series of nozzles (jets) located in a horizontal plane in front of the page. An ink supply cavity, common to 40 ink nozzles and maintained at a selected pressure and temperature, enables large quantities of uniform copy to be recorded on a conventional teletypewriter paper. A high potential charge on the platen, located directly behind the paper, attracts a stream of ink at high velocity from the selected nozzle. In transit, the stream breaks up into tiny droplets which are individually guided (electrostatically) in a vertical and a horizontal plane to form each character --- one character every eight milliseconds at 1200 words per minute. The nozzles are selected sequentially to print an 80 character line.

PRINTER MODULE LAYOUT

The cabinet supports the nonimpact recording unit and its cover on an extendable panel (figure 12). A shelf directly below the panel is provided for certain data or auxiliary sets. A blank panel (except for a recessed control switch) replaces the data set when used on our P.D.P.8. All horizontal and vertical drive pulses, directing the excursion of each stream of ink, are generated by one of four modules housed in the lower section of the cabinet. A self-contained multivoltage power supply furnishes the operating potential for the various logic circuits of the system and initiates the high potential fields for the respective elements of the printer. The memory logic is contained in the character generated module with facilities for changing from Baudot to ASCII code or vice versa. The interface module houses the terminal control logic, etc.

Facilities for supplying a large volume of teletypewriter paper to

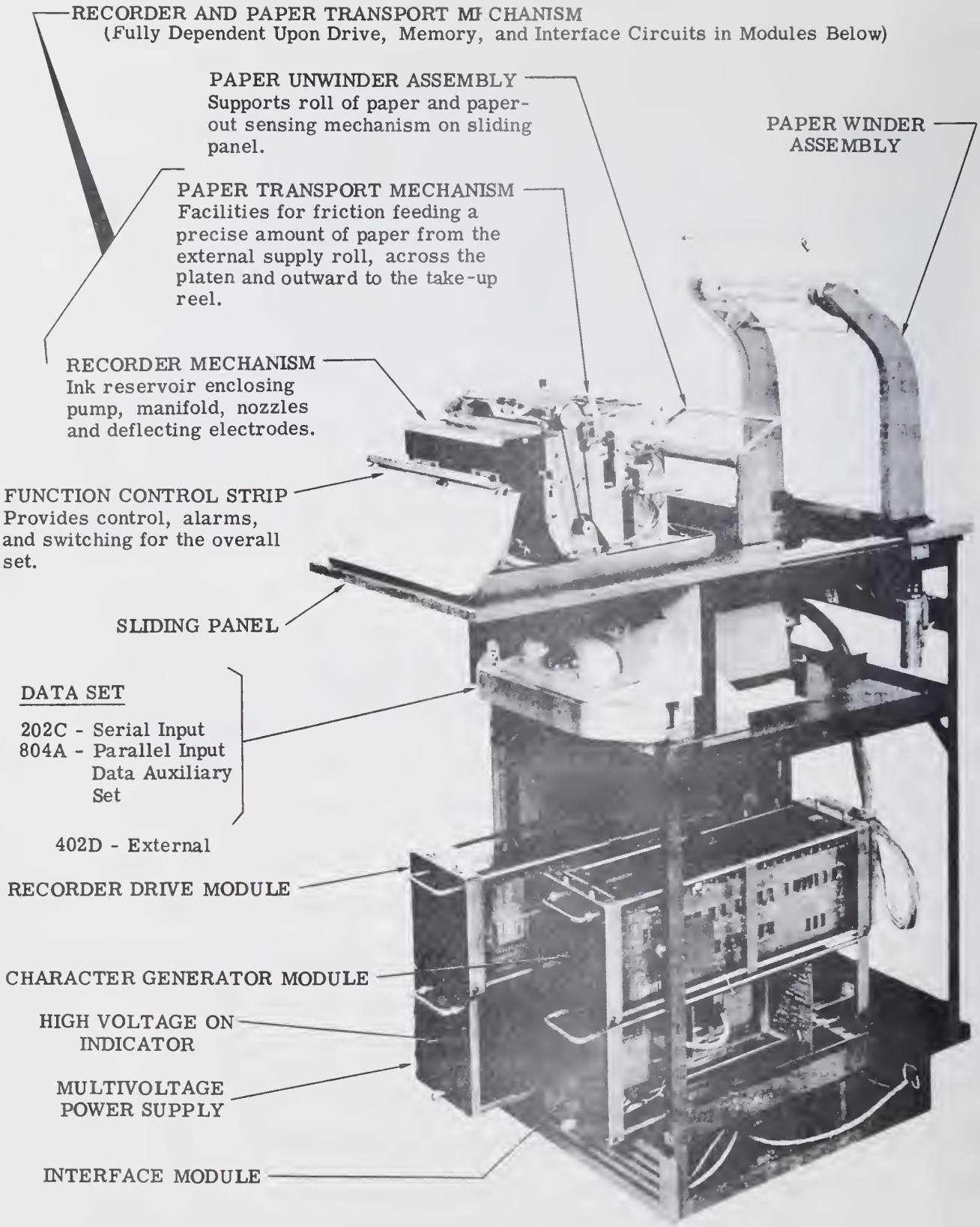


Figure 12
Inktronic Printer

the printer at high speeds and a motor driven take-up reel to retrieve the printed copy from the unit are provided by the external paper handling devices at the rear of the cabinet.

DESCRIPTION

The high speed page recorder and transport (figure 12) is capable of printing copy at any rate of speed up to 1200 words per minute. Unlike most telegraphic printing devices, this unit utilizes high potential fields to transfer ink to the paper and, with the exception of paper feeding, line feeding, and ink circulating (pump mechanisms, it has no moving parts.

The nonimpact printing function is dependent not only upon the initiation of a high velocity stream of ink from the selected nozzle, but also upon the direction of this trace to form a character. Printing takes place from left to right across the page under control of the recorder drive circuits. The recorder drive circuits control the flow of ink with the valving electrode as well as the forming of characters with the horizontal and vertical deflection electrodes. The maximum length of line is 80 characters.

Paper for the recorder and transport is fed from a 4-1/2 inch diameter roll, through the paper transport mechanism, to the line feed mechanism which controls the paper as it passes the ink nozzles. The paper tensioner assembly pulls the printed paper from the platen and also keeps it tightly against the platen during printing.

Illumination of the printing station is provided by a fluorescent lamp assembly attached toward the front of the cover. The plastic lens directs the light over the full width of the copy to be viewed.

The printing portion of the nonimpact page recorder consists of an ink tank with a means of maintaining consistent pressure on 40 ink nozzles, and a series of (four-element) electrodes to initiate and control the ink

stream. The platen, which attracts the ink from the respective nozzles, is located on the paper transport unit. The ink tank, enclosing the electrodes and ink handling components, extends across the entire width of the unit, and forms the front side of the paper transport mechanism.

The supply tank at the front of the unit has a liquid ink capacity of about one bottle of "INKTRONIC" ink TP301168 (12 ounces per bottle). The manifold, with its 40 nozzles and attached character forming electrodes, is located near the top of the tank and aligns with the platen. A continuous flow of ink is forced into the manifold reservoir by a diaphram type pump. The reservoir spillway maintains a certain ink level and enables the excess ink to be returned to the tank. Individual ducts connect the common reservoir with the respective nozzle. An electric heating element, embedded in the manifold below the nozzles, warms the liquid to facilitate an even flow of ink and the printing of a legible copy.

PRINTING

The recorder assembly consists of forty sets of printing units. Each printing unit consists of a nozzle, a valving electrode, a pair of vertical deflection electrodes, and a pair of horizontal deflection electrodes. Across the front of the print head assembly is the mask. There is a rectangular hole in the mask in front of each printing unit. Each printing unit prints two characters, one in a left matrix and one in a right matrix. A maximum of 32 points in the matrix are available for forming one character. However, one of these points must be used to end the character. Therefore, 31 points in the matrix are the maximum area available for the actual printing of one character (figure 13).

The manifold supports the nozzles and provides a supply of ink to each of the forty nozzles. The manifold and nozzles are held at a constant negative voltage of -1900 v dc.

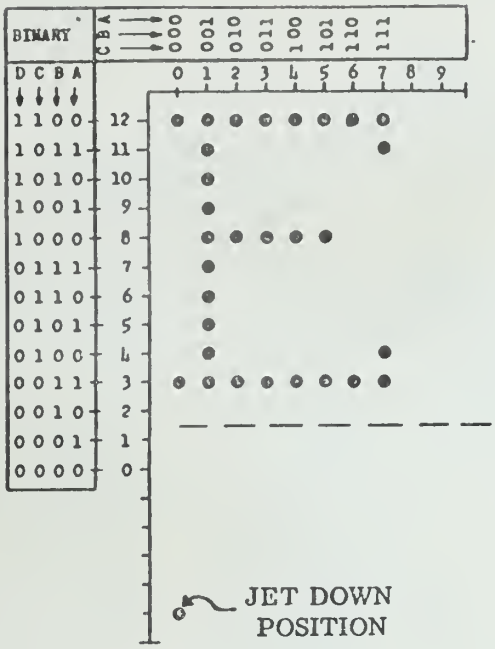


Figure 13
Matrix Pattern

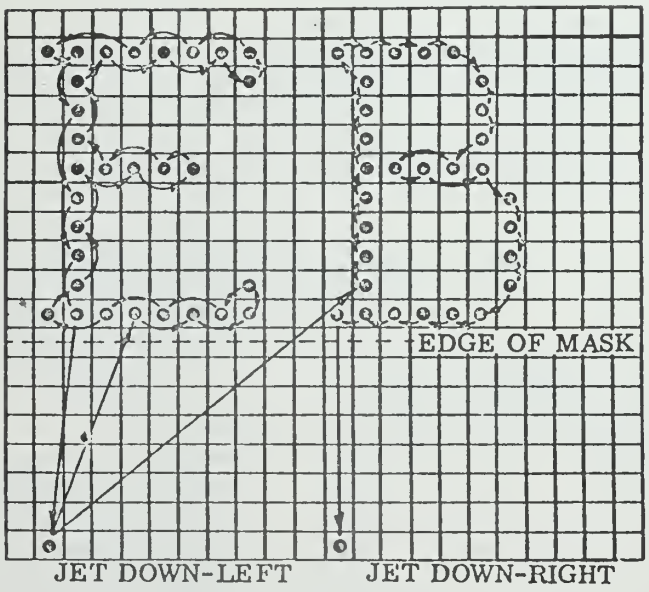


Figure 14
Basic Tracing Pattern of Typical Electrode Assembly

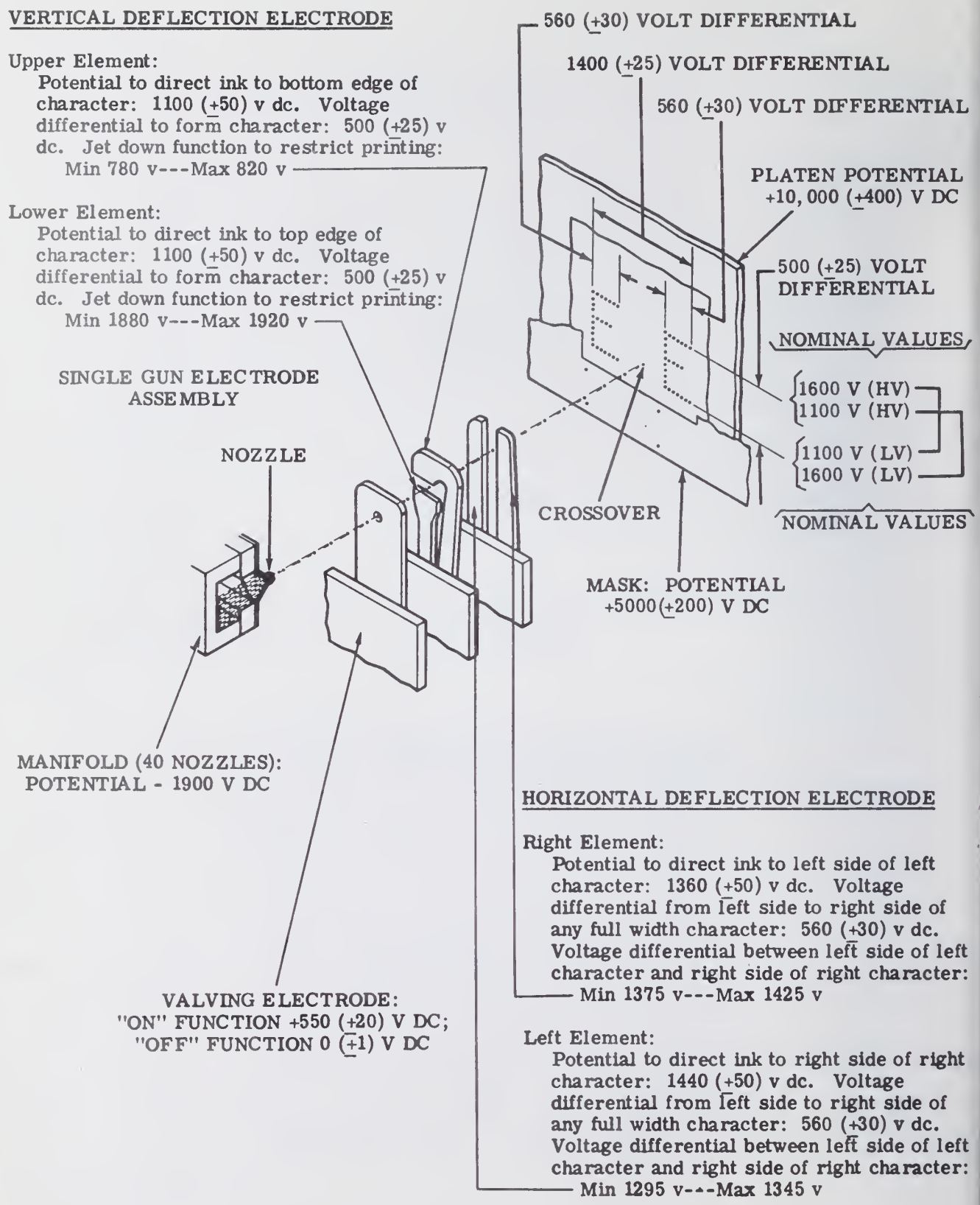


Figure 15
Nominal Electrode Voltages

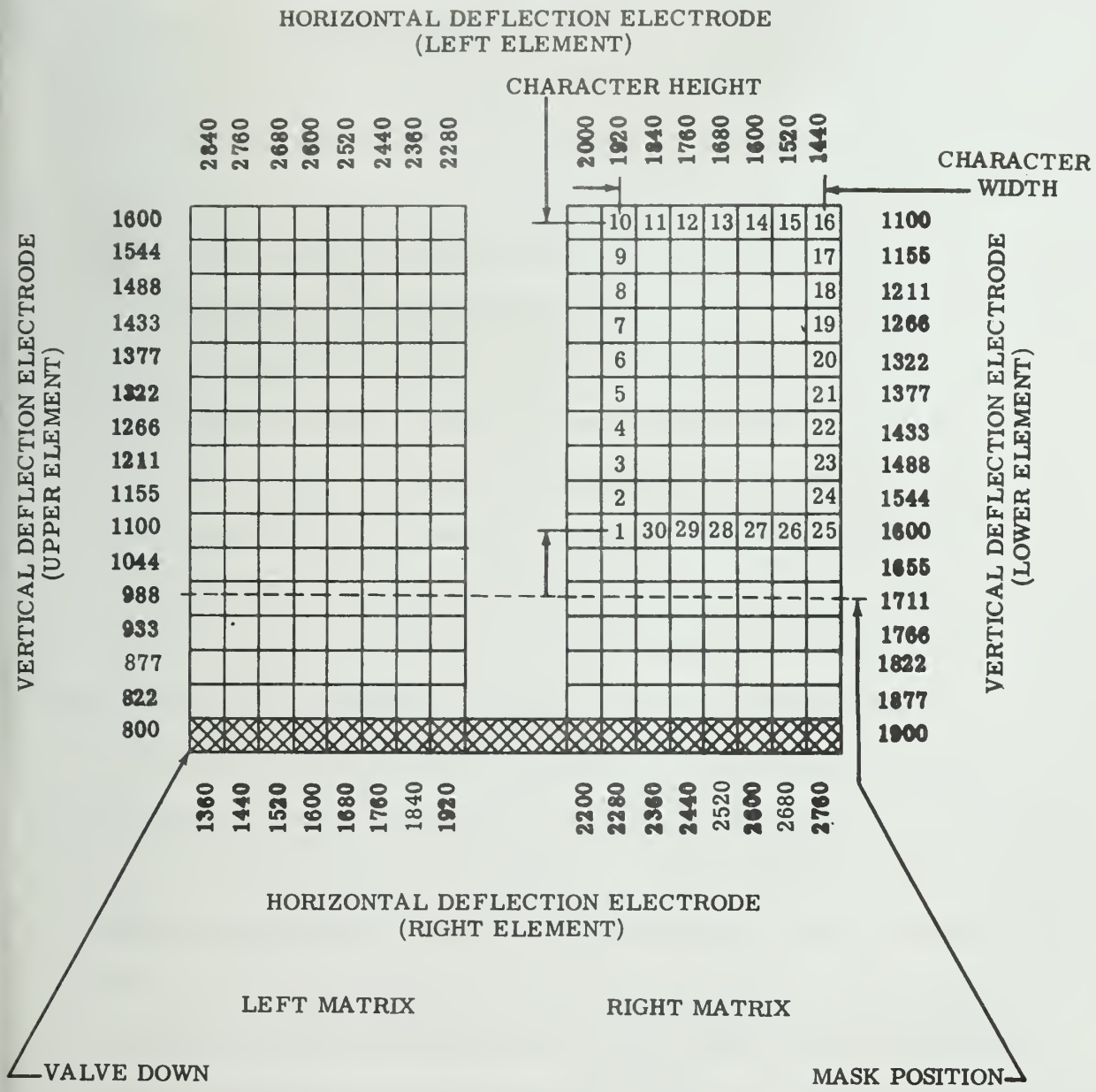


Figure 16
Character Matrix and Deflection Voltage

The valving electrode, in front of each nozzle, controls the flow of ink from that nozzle. The valving electrode derives its potential of +550 v dc (figure 15) from the spacing drive power supply contained in cabinet. The spacing drive power supply uses the input signals, received from the character generator, to select the appropriate valving electrodes which will turn on the appropriate nozzles for printing. When the valving electrode is at the off voltage (0 v dc), no ink issues from the nozzle. When it is at the on voltage (+550 v dc), ink is extracted from the nozzle in the form of a droplet stream. The droplets, approximately 0.001 inches in diameter, pass through the hole in the valving electrode and proceed with increasing velocity to the region of the deflection electrodes.

The first pair of deflection electrodes which influence the path of the ink droplets are the vertical deflection electrodes. These electrodes are supplied with their deflection voltage (figure 15) by the high voltage power supply which is modulated by the digital-to-analog converter for vertical printing contained in lower cabinet. The vertical deflection electrodes, one above and one below the jet, are arranged to form a horizontal slot. If the upper electrode is at a higher voltage than the lower, the ink droplets will be deflected upward; or conversely, if the lower electrode is at a high voltage than the upper, the path of the droplets will be deflected downward. The average voltage of these two electrodes is higher than that of the valving electrode; therefore, the droplets are accelerated.

The next set of electrodes, the horizontal deflection electrodes, are arranged to form a vertical slot. These electrodes are supplied with their deflection voltage (figure 12) by the high voltage power supply (contained in the lower cabinet) which is modulated by the digital-to-analog converter for horizontal printing. Similar to the above description, the

droplets can be deflected horizontally by varying the electrode voltage. The average voltage of this electrode set is higher than the previous set; so, again the ink droplets are accelerated.

In their flight toward the paper, the ink droplets encounter one more electrode, the mask. The mask derives its constant +5000 v dc (figure 15) from the power supply located at the rear of the paper handler. When a nonprinting condition exists, the mask acts as a shield. That is, the voltage at the deflection electrodes is such that the stream of ink droplets are deflected downward striking the lower portion of the mask. The ink droplets are therefore prevented from continuing their journey to the paper and drain down the mask to be returned to the ink supply in the manifold. When a printing condition exists, the voltage is selected to hold the mask voltage at the same average voltage established by the electric field between the previous electrode set and the platen. As far as the ink droplets are concerned, the mask is invisible. Also the mask provides some protection for the deflecting electrodes.

A fixed amount of time is available for printing each character. At 1200 words per minute this is 8 milliseconds. However, characters built up from relatively few dots in the matrix pattern, such as the letter I will be finished printing early and a wait period occurs. Even though the ink jet is turned on, it must not print. This is accomplished by deflecting the ink jet downward to a considerable distance below the printing area where it strikes the mask shown in figure 16. Ink that hits the mask cannot reach the paper, so deflecting the ink downward is equivalent, in effect, to turning off the ink jet. Whenever a jet is turned on by the valving electrode (ink flowing) but is not printing, it is directed toward the mask. This situation occurs at three different

times in the printing process: first, during the time allowed for ink to start flowing, but before printing has begun; second, after a left character has been printed but before a right character has started; and third, after printing has been completed and during the time allowed to turn off the ink jet.

To print a line of characters from left to right, each of the 40 ink jets could be turned on in successize order. Thus, the first jet could be turned on, print two characters followed by the second jet to print the next two characters, and so forth. Each individual jet prints first a left and then a right character until the entire line is printed. The return to starting position for a new line is called reset and is initiated by a CARRIAGE RETURN (reset) signal.

To understand the character signals which must be supplied as input signals to the printer drive for providing the required vertical and horizontal deflection at the electrodes, refer to figure 13. This basic matrix pattern shows 12 possible positions above the zero position. The seven horizontal positions are represented by a 3-bit binary code, as shown above the matrix pattern. Any position in the matrix pattern may be located by specifying four vertical bits and three horizontal bits.

DISPLAY PROCESSING UNIT

The Display Processing Unit (DPU) is the interface between the PDP8 memory and the remainder of a display system. (The display system configuration is shown in Figure 17). Because this interface executes programs from memory, because it has an instruction repertoire, and because programs can be written for the display processor, it can be thought of as a computer. It is a special kind of computer with capabilities oriented toward making pictures rather than performing computational tasks. Many of its instructions are descriptive of drawing operations rather than computational operations. Because the DPU operates in conjunction with a general purpose computer, "general" computing capabilities were not given to it. The DPU fetches data from the PDP8 core memory, decodes it and generates picture information. This information is then transferred via a core memory buffer to a track of the central disk buffer, thus releasing the DPU for other tasks. The DPU performs the same functions that the DEC 338 does, with the additional capabilities of controlling and refreshing the picture at as many as 16 display terminals. All commands are transferred to the DPU via the PDP8 single cycle data-break system. The programmer may specify which terminal he wishes to access at any time.

A special hardware scheme is used to generate the incremental commands from the combinations of codes which form lines and characters.

The order of execution of all the Control State instructions, PDP8 display oriented instructions and the picture generation, is determined by a central control unit. The unit is composed of several sequential control points which govern the data flow in the DPU.

An interrupt queueing scheme controls the data communication between the display terminals and the DPU.

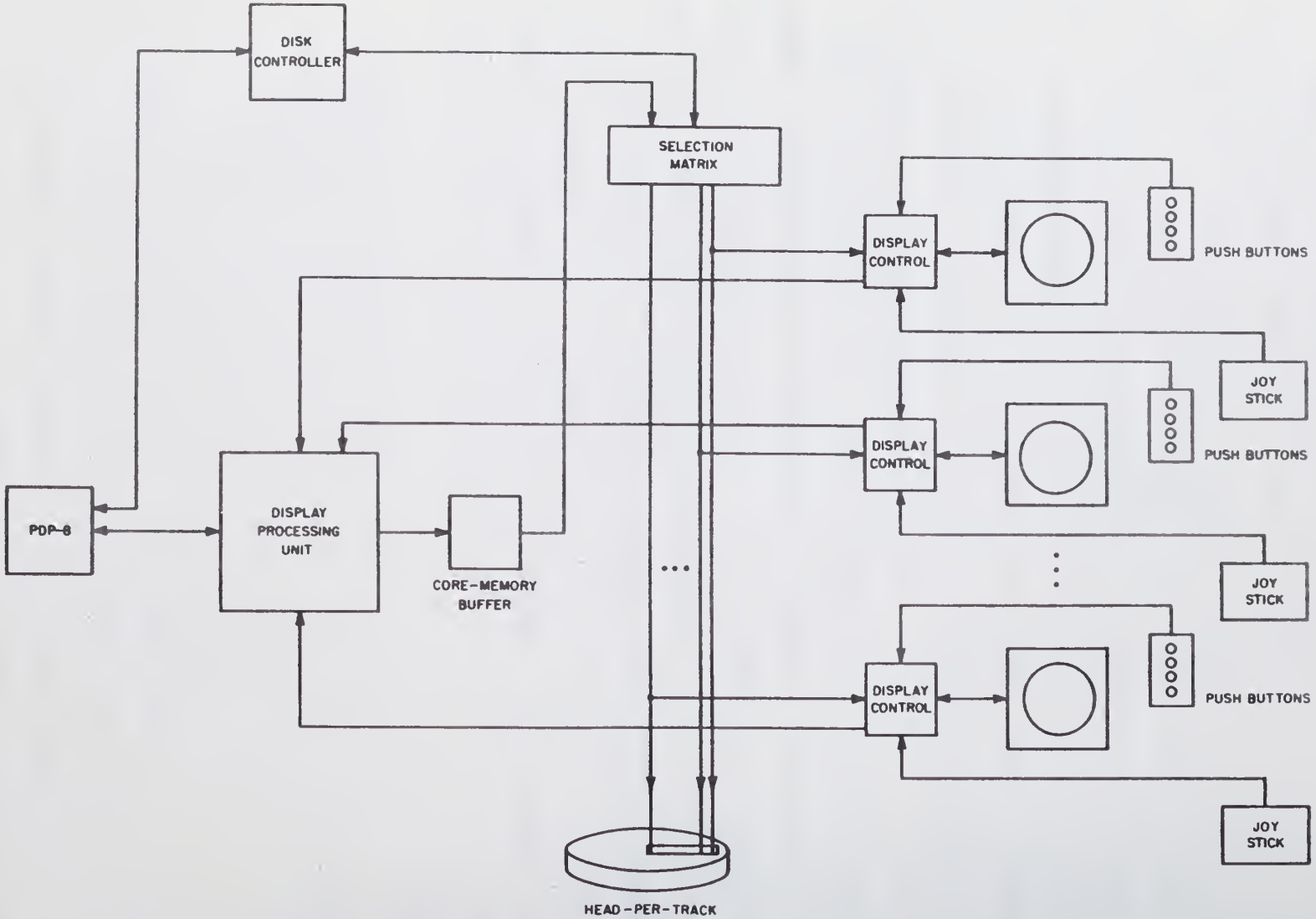


Figure 17

Display System Configuration

A central disk buffer holds the picture information for up to 16 display terminals, with a single track of the disk being dedicated to each of the terminals. Each of the tracks has its own read-head and line driver. The disk rotates at 30 revolutions per second, so the picture on each scope is refreshed at 30-cycle rate. This rate is high enough to give a flicker-free display. At the data rate used, 10^6 points/second are plotted by the display terminals.

The picture on each track of the disk is specified in terms of simple 3-bit incremental command. These commands are decoded by a display control at each of the scope terminals where X-Y deflection signals are produced to position and display points. The commands allow the beam to be moved a certain number of units in any direction on a 1024 x 1024 grid (left-right, up-down, or diagonally) covering a 10" x 10" area on the scope face.

Information corresponding to the initial values of X and Y, four spot intensities, scale factor, P. B. enable, and joystick interrupt-enable are also stored on the disk. Zoom option information is transferred directly to the display terminal, so that frames may be expanded by a factor of two, four, or eight.

The operator of the CRT display can communicate immediately with the DPU and the PDP8 processor by using the incremental joystick or the push-button control box.

The DEC 338, in order to generate typical pictures, uses about 30,000 moves per frame, and the picture has to be reconstructed and regenerated 30 times per second to avoid excessive flicker. Also, the 338 may access the PDP8 via the data-break system only once in three

PDP8 memory cycles, degrading the speed of generating points and vectors which results in lower picture capacity. The DPU disk buffer contains about 100,000 bits or 33,000 instructions in a full track. A track of data corresponds to a picture containing 660" of drawings. This means 66 screen widths of horizontal or vertical lines (in scale of 2) or about 1500 characters, or a proportional mix.

Consequently, the DPU disk configuration with its independent picture refreshing capability, easily handles display files like those executed by the DEC 338.

Data Disk

6551		Gate AC to Address Register
6552		Clear Disk Done and Interrupt Enable
6554		Enable Interrupt
6561		Skip on Disk Done
6562		Transfer AC contents to Disk Control
6564		

DECTAPE

6761	DTRA	Read Status Register A
6762	DTCA	Clear Status Register A
6764	DTXA	Load Status Register A
6771	DTSF	Skip On Flags
6772	DTRB	Read Status Register B
6774	DTLB	Load Status Register B

DISPLAY

6051	RPDP	Read Push Down Pointer
6052	RXP	Read X Position Register, bits 1-12
6054	RYP	Read Y Position Register, bits 1-12
6061	RDAC	Read Display Address Counter
6062	RS1	Read Status 1
6064	RS2	Read Status 2
6071	RPB	Read Push Buttons
6072	RSG1	Read Slave Group 1
6074	RSG2	Read Slave Group 2
6132	SLLP	Skip on Light Pen Hit Flag
6135	SPDP	Set the Push Down Pointer
6142	SPSP	Skip on Slave Light Pen Hit Flag
6145	SIC	Set Initial Conditions
6151	SPES	Skip on External Stop Flag
6152	SPEF	Skip on Edge Flag
6154	STPD	Stop Display (External)
6155	LBF	Load Break Field
6161	CFD	Clear Display Flags
6162		
6164	RES2	Resume After Stop Code
6165	INIT	Initialize the Display
6171	SPSF	Skip on Internal Stop Flag
6172	SPMI	Skip on Manual Interrupt
6174	RES1	Resume after Light Pen Hit, Edge, or External Stop Flag
6303	SCG	Set Character Generator
6304	RCG	Read Character Generator
6311		Skip if Clock Flag = 0
6312		Clear Clock Flag and Enable Clock Interrupt
6314		Disable Clock Interrupt

EXTENDED MEMORY

6201	CDF0	Change to Data Field 0
6202	CIF0	Change to Instruction Field 0
6204		
6211	CDF1	Change to Data Field 1
6212	CIF1	Change to Instruction Field 1
6214	RDF	Read Data Field
6221	CDF2	Change to Data Field 2
6222	CIF2	Change to Instruction Field 2
6224	RIF	Read Instruction Field
6231	CDF3	Change to Data Field 3
6232	CIF3	Change to Instruction Field 3
6234	RIB	Read Interrupt Buffer
6241	CDF4	Change to Data Field
6242	CIF4	Change to Instruction Field 4
6244	RMF	Restore Memory Field
6251	CDF5	Change to Data Field 5
6252	CIF5	Change to Instruction Field 5
6254		
6261	CDF6	Change to Data Field 6
6262	CIF6	Change to Instruction Field 6
6264		
6271	CDF7	Change to Data Field 7
6272	CIF7	Change to Instruction Field 7
6274		

ILLIAC III

6731	Skip on Device Ready
6732	Clear Device Ready, Information Ready
6734	Clear Data Ready
6741	Skip on Data Ready
6742	Gate Contents of AC and Data Accepted
6744	External Device Comp.
6751	
6752	
6754	

INKTRONIC

6441	Skip on Printer Ready
6442	Enable Interrupt
6444	Disable Interrupt
6451	Skip on Character Done
6452	Clear Character Done
6454	Gate Character and Start Print

Interface to 630

6631		Skip on Flags
6632		Clear AC and Receiver Flag
6634		Gate Receiver Output to AC
6641		Clear Interrupt Enable
6642		Set Interrupt Enable
6644		Clear Transmitter Flag and Input Data from AC

MUSIC MAKER

6701		Reset both flip flops to "0"
6702		Complements flip flop "1"
6704		Complements flip flop "2"

PDA-2701

6401	ICR1	Initiate Channel Read
6402	ICR2	Gate Contents of AC into Data Address Register
6404	ICR4	(not used)
6411	SRR	Skip on Read Ready
6412	ERI	Enable Read Interrupt
6414	CRD	Clear Read Done
6421	SRD	Skip on Read Done
6422	DRI	Disable Read Interrupt
6424	SWCR	Set Word Count Register
6431	SPE	Skip on Parity Error
6432	CPE	Clear Parity Error
6434	SEM	Set Extended Memory
6501	ICW1	Initiate Channel Write
6502	ICW2	Gate Contents of AC into Data Address Register
6504	ICW4	(not used)
6511	SWR	Skip on Write Ready
6512	EWI	Enable Write Interrupt
6514	CWD	Clear Write Done
6521	SWD	Skip on Write Done
6522	DWI	Disable Write Interrupt
6524		(not used)

PROGRAM INTERRUPT

6001	ION	Turn Interrupt On
6002	IOF	Turn Interrupt Off

SYLVANIA TABLET

6711		Skip on Tablet Ready
6712		Disable Interrupt and Clear Data Ready
6714		Enable Interrupt
6721		Read Tablet "X"
6722		Read Tablet "Y"
6724		Read Tablet "Z"

TELETYPE-KEYBOARD/READER

6031	KSF	Skip if Keyboard/Reader Flag = 1
6032	KCC	Clear AC and Keyboard/Reader Flag
6034	KRS	Read Keyboard/Reader Buffer, Static
6036	KRB	Clear AC, read Keyboard/Reader Buffer and Clear Keyboard Flag

TELETYPE-TELEPRINTER/PUNCH

6041	TSF	Skip if Teleprinter/Punch Flag = 1
6042	TCF	Clear Teleprinter/Punch Flag
6044	TPC	Load Teleprinter/Punch Buffer, Select and Print
6046	TLS	Load Teleprinter/Punch Buffer, Select and Print, and Clear Teleprinter/Punch Flag

6001 ION	6101
6002 IOF	6102
6004 ADC	6104
6011 Save for high speed reader	6111
6012 "	6112
6014 "	6114
6021 Save for high speed punch	6121
6022 "	6122
6024 "	6124
6031 TTY Reader	6131 338
6032 "	6132 "
6034 "	6134 "
6041 TTY Printer	6141 "
6042 "	6142 "
6044 "	6144 "
6051 338	6151 "
6052 "	6152 "
6054 "	6154 "
6061 "	6161 "
6062 "	6162 "
6064 "	6164 "
6071 "	6171 "
6072 "	6172 "
6074 "	6174 "

6201 Extended Memory	6301 Type VC38 Character Generator
6202 "	6302 "
6204 "	6304 "
6211 "	6311 338 Real Time Clock
6212 "	6312 "
6214 "	6314 "
6221 "	6321
6222 "	6322
6224 "	6324
6231 "	6331
6232 "	6332
6234 "	6334
6241 "	6341
6242 "	6342
6244 "	6344
6251 "	6351
6252 "	6352
6254 "	6354
6261 "	6361
6262 "	6362
6264 "	6364
6271 "	6371
6272 "	6372
6274 "	6374

6401	PDP-8 to 2701	6501	PDP-8 to 2701
6402	"	6502	"
6404	"	6504	"
6411	"	6511	"
6412	"	6512	"
6414	"	6514	"
6421	"	6521	"
6422	"	6522	"
6424	" (not used)	6524	" (not used)
6431	PDP-8 to 2701	6531	
6432	"	6532	
6434	"	6534	
6441	Inktronic Printer	6541	
6442	" "	6542	
6444	" "	6544	
6451	" "	6551	Data Disk
6452	" "	6552	"
6454	" "	6554	"
6461		6561	"
6462		6562	"
6464		6564	"
6471		6571	
6472		6572	
6474		6574	

6601	6701 Music Maker
6602	6702 "
6604	6704 "
6611	6711 Sylvania Tablet
6612	6712 "
6614	6714 "
6621	6721 "
6622	6722 "
6624	6724 "
6631 PDP-8 Interface to 630	6731 ILLIAC III
6632 "	6732 "
6634 "	6734 "
6641 "	6741 "
6642 "	6742"
6644 "	6744 "
6651	6751 "
6652	6752 "
6654	6754 "
6661	6761 DECTAPE
6662	6762 "
6664	6764 "
6671	6771 "
6672	6772 "
6674	6774 "

Form AEC–427
(6/68)
AECM 3201

U. S. ATOMIC ENERGY COMMISSION

UNIVERSITY–TYPE CONTRACTOR'S RECOMMENDATION FOR DISPOSITION OF SCIENTIFIC AND TECHNICAL DOCUMENT

(See Instructions on Reverse Side)

1. AEC REPORT NO.	2. TITLE
COO-1469-0151	Graphics 8 Graphics Hardware - 1469 Gear

3. TYPE OF DOCUMENT (Check one):

- [X] a. Scientific and technical report
- [ ] b. Conference paper not to be published in a journal:
  - Title of conference _____
  - Date of conference _____
  - Exact location of conference _____
  - Sponsoring organization _____
- [ ] c. Other (Specify) _____

4. RECOMMENDED ANNOUNCEMENT AND DISTRIBUTION (Check one):

- [X] a. AEC's normal announcement and distribution procedures may be followed.
- [ ] b. Make available only within AEC and to AEC contractors and other U.S. Government agencies and their contractors.
- [ ] c. Make no announcement or distrubution.

5. REASON FOR RECOMMENDED RESTRICTIONS:

6. SUBMITTED BY: NAME AND POSITION (Please print or type)

C. W. Gear
Principle Investigator

Organization

Department of Computer Science
University of Illinois
Urbana, Illinois 61801

Signature	Date
Charles W Gear.	December 24, 1969

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7. AEC CONTRACT ADMINISTRATOR'S COMMENTS, IF ANY, ON ABOVE ANNOUNCEMENT AND DISTRIBUTION RECOMMENDATION:

8. PATENT CLEARANCE:

- [ ] a. AEC patent clearance has been granted by responsible AEC patent group.
- [ ] b. Report has been sent to responsible AEC patent group for clearance.
- [ ] c. Patent clearance not required.